

初定规格 Preliminary specification

正式规格 Official specifications

SPI/MCU 信号转 TTL 信号模块 用户手册

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本模块提供 SPI 与 8/16 位 MCU 并口界面, 内建 128Mb 显示内存, 可以推动 16bits(5/6/5) 或是 24bits(8/8/8) RGB 接口的 TFT 显示屏, 并达到 Alpha RGB: 8888 颜色深度。

This module provides SPI and 8/16-bit MCU parallel interface, with built-in 128Mb display memory, capable of driving 16bits (5/6/5) or 24bits (8/8/8) RGB interface TFT displays, achieving Alpha RGB: 8888 color depth.

一、特点 Feature :

1) 电源电压: 3.0V±0.3;

Power supply voltage: 3.0V±0.3

2) 支持 SPI 串口与 8/16 位 MCU 并口界面;

Supports SPI serial port and 8/16-bit MCU parallel port interface;

3) 内建 JPG 硬件解码器;

Built-in JPG hardware decoder;

4) 支持 1024*768 分辨率内的 16/24bits RGB 接口显示屏、色彩 α RGB 8:8:8:8 显示数据;

Supports 16/24bits RGB interface displays within 1024*768 resolution, with color α RGB 8:8:8:8 display data;

5) 支持镜像和垂直翻转显示功能;

Supports mirroring and vertical flipping display functions;

6) 内建大容量 128Mb 显示内存, 支持多重显示, 在显示缓冲区切换主显示视窗;

Built-in high-capacity 128Mb display memory, supports multiple displays, and switches the main display window in the display buffer;

7) 内建几何绘图引擎, 支持画点、画线、画曲线、椭圆、三角形、矩形、圆角矩形等功能;

Built-in geometric drawing engine, supporting functions such as drawing points, lines, curves, ellipses, triangles, rectangles, and rounded rectangles;

8) 内建 2D BitBLT 图形加速引擎, 提供带 ROP 光栅运算的复制图像显示功能、PIP (Picture-in-Picture) 功能及图形混合透明显示功能;

Built-in 2D BitBLT graphics acceleration engine, providing copy image display function with ROP raster operation, PIP (Picture-in-Picture) function, and graphics blending transparent display function;

9) 工作温度范围: -40°C~85°C;

Operating temperature range: -40°C to 85°C;

三、引脚说明

3.1 MCU+SPI 接口输入引脚说明 Description of MCU+SPI interface input pins

引脚编号 Pin NO.	标号 Symbol	详细描述 Description
1	WAIT	等待输出信号 Waiting for output signal 当 MCU 对 模块进行读写控制时, 如果模块处于忙碌状态, 会将 WAIT# 变成低电位, 用来告知 MCU 进入等待周期, 不用时不联接; When the MCU performs read and write control on the module, if the module is busy, it will change WAIT# to a low voltage to inform the MCU to enter a waiting period, Don't connect when not in use;
2	INT	中断输出信号 Interrupt output signal 当设定的中断条件发生, 此引脚变成低电位, 用来产生一中断输出告知 MCU, 不用时不联接; When the set interrupt condition occurs, this pin becomes low potential, which is used to generate an interrupt output to inform the MCU. It is not connected when not in use;
3~4	NC	不连接 Not connected
5~6	LEDA	LED阳极 LED anode
7~8	LEDK	LED阴极 LED cathode
9	NC	不连接 Not connected
10	TP-VDD	数字电源电压 Digital supply voltage
11	TP-SDA	TP-IIC 数据信号 TP-IIC data signal
12	TP-SCL	TP-IIC 时钟信号 TP-IIC clock signal
13	GND	电源地 Power supply ground
14	TP-INT	TP 中断信号 TP Interrupt signal
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引脚编号 Pin NO.	标号 Symbol	详细描述 Description
15	TP-RTN	TP 重置复位引脚。 TP Reset pin.
16	GND	电源地 Power supply ground
17~24	DB[15~8]	16位并行接口中, DB[0~15]被用作数据总线;8位并行接口中, DB[0~7]被用作数据总线; In a 16-bit parallel interface, DB[0~15] is used as the data bus; in an 8-bit parallel interface, DB[0~7] is used as the data bus; 在 SPI 模式时, DB[15~8]被用作 GPIO 信号; In SPI mode, DB[15~8] is used as a GPIO signal;
25	DB7 SPI-SCLK	并口模式时, DB[7]被用作数据总线; SPI 模式时, DB[7]被用作串口时钟信号; In parallel port mode, DB[7] is used as the data bus; In SPI mode, DB[7] is used as the serial port clock signal;
26	DB6 SPI-SDI	并口模式时, DB[6]被用作数据总线; 4 线 SPI 模式时, DB[6]被用作数据输入;在 3 线 SPI 模式下未被使用, 请接到地 (GND)。 In parallel port mode, DB[6] is used as the data bus; In 4-wire SPI mode, DB[6] is used as a data input; in 3-wire SPI mode, it is not used and should be connected to ground (GND).
27	DB5 SPI-SD0(4L) SPI-SD(3L)	并口模式时, DB[5]被用作数据总线; SPI 模式时, DB[5]被用作4 线 SPI 数据输出;在 3 线 SPI 模式下用作双向数据引脚。 In parallel port mode, DB[5] is used as the data bus; In SPI mode, DB[5] is used as a 4-wire SPI data output; in 3-wire SPI mode, it is used as a bidirectional data pin.
28	DB4 SPI-CSX	并口模式时, DB[4]被用作数据总线; 在 SPI 模式时, DB[4]被用作 SPI 片选信号; In parallel port mode, DB[4] is used as the data bus; In SPI mode, DB[4] is used as the SPI chip select signal;
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引脚编号 Pin NO.	标号 Symbol	详细描述 Description
29	DB3	<p>并口模式时，DB[3]被用作数据总线； 4 线 SPI 模式时，此引脚被设置为高电位；在 3 线 SPI 模式下未被使用，请接到地（GND）。</p> <p>In parallel port mode, DB[3] is used as the data bus; In 4-wire SPI mode, this pin is set to high potential; in 3-wire SPI mode, it is not used and should be connected to ground (GND).</p>
30~32	DB[2~0]	<p>并口模式时，DB[2~0]被用作数据总线； 在 SPI 模式时，DB[2~0]被用作 GPIO 信号；</p> <p>In parallel port mode, DB[5] is used as the data bus; In SPI mode, DB[2~0] is used as a GPIO signal;</p>
33	RESX	<p>复位输入信号。信号为低电平时并且维持大于 32 个时钟周期长度，模块将产生复位动作。</p> <p>Reset input signal. When the signal is at a low level and maintains a duration of more than 32 clock cycles, the module will initiate a reset action.</p>
34	RD	<p>在 8080 并口模式，此引脚为"RD"信号，RD = 0，代表 MCU 对模块进行数据读取或是状态读取周期；在串口模式，则此脚位可以设置为GPIB[1]，有内部拉高电阻。</p> <p>In the 8080 parallel port mode, this pin serves as the "RD" signal, where RD = 0 indicates that the MCU is performing a data read or status read cycle on the module. In the serial port mode, this pin can be set to GPIB[1] and features an internal pull-up resistor.</p>
35	WR	<p>在 8080 并口模式，此引脚为"WR"信号，WR = 0，代表 MCU 对模块进行命令写入或是数据写入周期；在串口模式，则此脚位可以设置为GPIB[2]，有内部拉高电阻。</p> <p>In the 8080 parallel port mode, this pin serves as the "WR" signal, where WR = 0 indicates that the MCU is performing a command write or data write cycle to the module. In the serial port mode, this pin can be set to GPIB[2] and features an internal pull-up resistor.</p>
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引脚编号 Pin NO.	标号 Symbol	详细描述 Description
36	RS	<p>在 8080 并口模式，此引脚为"RS"信号。RS = 0，代表 MCU对模块进行命令写入周期；RS = 1，代表 MCU对模块进行数据写入周期；在串口模式，则此脚位可以设置为GPIB[3]，有内部拉高电阻。</p> <p>In 8080 parallel port mode, this pin serves as the "RS" signal. When RS = 0, it indicates that the MCU is performing a command write cycle to the module; when RS = 1, it signifies that the MCU is executing a data write cycle to the module. In serial port mode, this pin can be set to GPIB[3] and features an internal pull-up resistor.</p>
37	CS	<p>在 8080 并口模式，此引脚为"CS"信号。CS = 0，代表 MCU对模块进行命令或是数据读写；在串口模式，则此脚位可以设置为GPIB[0]，有内部拉高电阻。</p> <p>In the 8080 parallel port mode, this pin serves as the "CS" signal. When CS = 0, it indicates that the MCU is issuing commands or performing data read/write operations on the module. In the serial port mode, this pin can be set to GPIB[0] and features an internal pull-up resistor.</p>
38~39	+3.3V	<p>3.3V 电源 3.3V Power supply</p>
40	GND	<p>电源地 Power supply ground</p>
- 结束 - - END -		

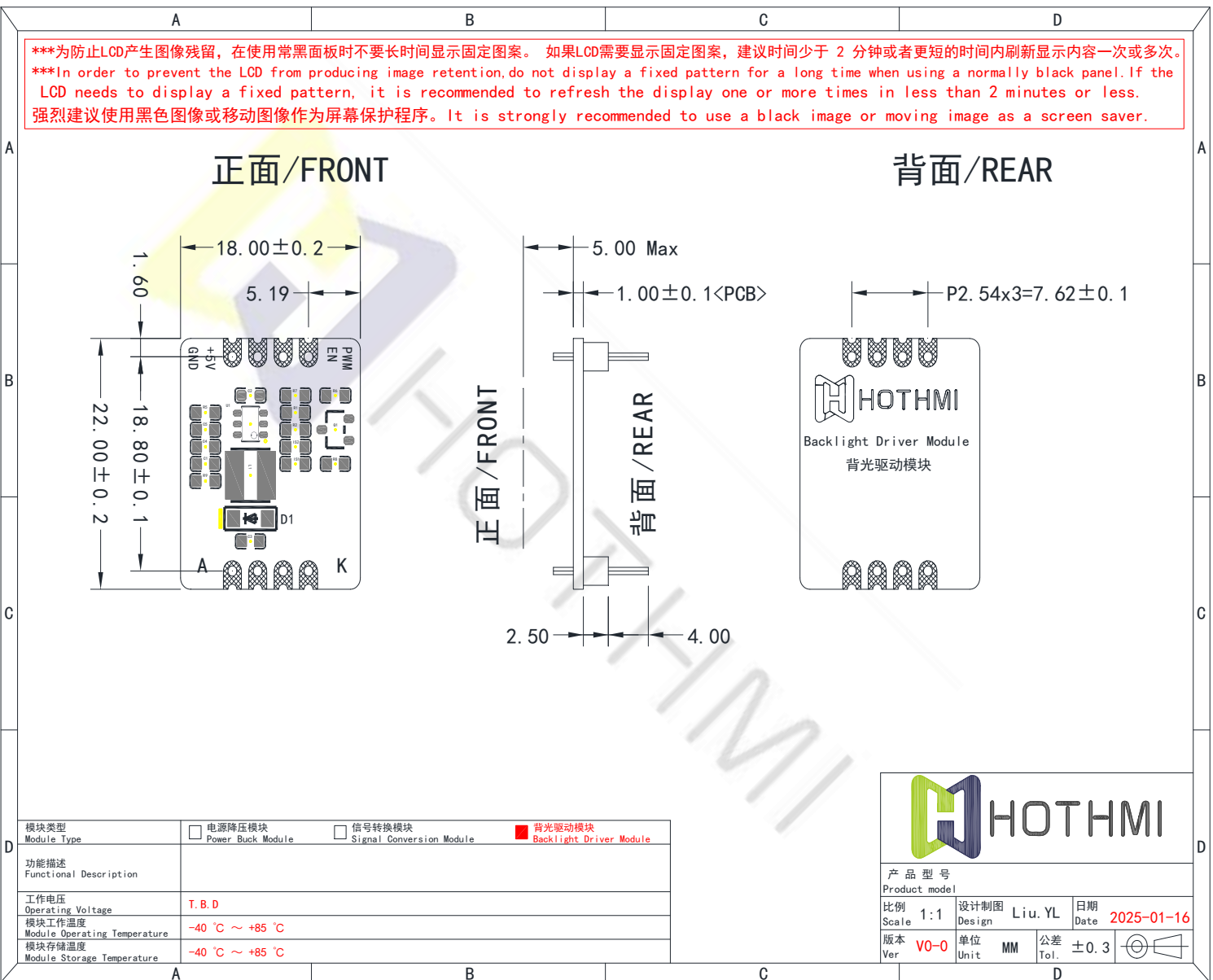
3.2 RGB 输出引脚说明 Description of RGB output pins

引脚编号 Pin NO.	标号 Symbol	详细描述 Description
1	LEDK	LED阴极 LED cathode
2	LEDA	LED阳极 LED anode
3	GND	电源地 Power supply ground
4	VCI	电源 Power supply
5~12	DR[0~7]	8位数据总线显示红色数据 The 8-bit data bus displays red data
13~20	DG[0~7]	8位数据总线显示绿色数据 8 bit data bus display green data
21~28	DB[0~7]	8位数据总线显示蓝色数据 The 8-bit data bus displays blue data
29	GND	电源地 Power supply ground
30	PCLK	像素时钟输入引脚 Pixel clock input pin
31	NC	不连接 Not connected
32	HSD	水平同步信号 Horizontal sync signal.
33	VSD	垂直同步信号 Vertical sync signal.
34	DEN	数据输入启用 Data input enable
35	RESX-1	显示面板复位信号，接电阻"R17"时有效 Display panel reset signal valid when connected to resistor "R17"
36	GND	电源地 Power supply ground
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引脚编号 Pin NO.	标号 Symbol	详细描述 Description
37	RESX-2 TP-RTN	<p>显示面板复位信号，电阻接"R16"时有效 Display panel reset signal valid when connected to resistor "R16"</p> <p>TP复位信号，接排阻"CTP"时有效 TP reset signal is valid when connected to the pull-up resistor "CTP"</p>
38	SPI-CS TP-INT	<p>显示面板SPI片选信号，接电阻"R11"时有效 The SPI chip select signal of the display panel is valid when connected to resistor "R11"</p> <p>TP 中断信号，接排阻"CTP"时有效 TP reset signal is valid when connected to the pull-up resistor "CTP"</p>
39	SPI-SCL TP-SCL	<p>显示面板SPI时钟信号，接电阻"R15"时有效 The SPI clock signal of the display panel is valid when connected to resistor "R15"</p> <p>TP IIC 时钟信号，接排阻"CTP"时有效 The TP IIC clock signal is valid when connected to the "CTP" resistor</p>
40	SPI-SDA TP-SDA	<p>显示面板SPI数据信号，接电阻"R14"时有效 The display panel SPI data signal is valid when connected to resistor "R14"</p> <p>TP IIC 数据信号，接排阻"CTP"时有效 TP IIC data signal is valid when connected to the "CTP" resistor</p>
<p>- 结束 - - END -</p>		

3.3 电容触摸引脚说明 CTP Pin Description

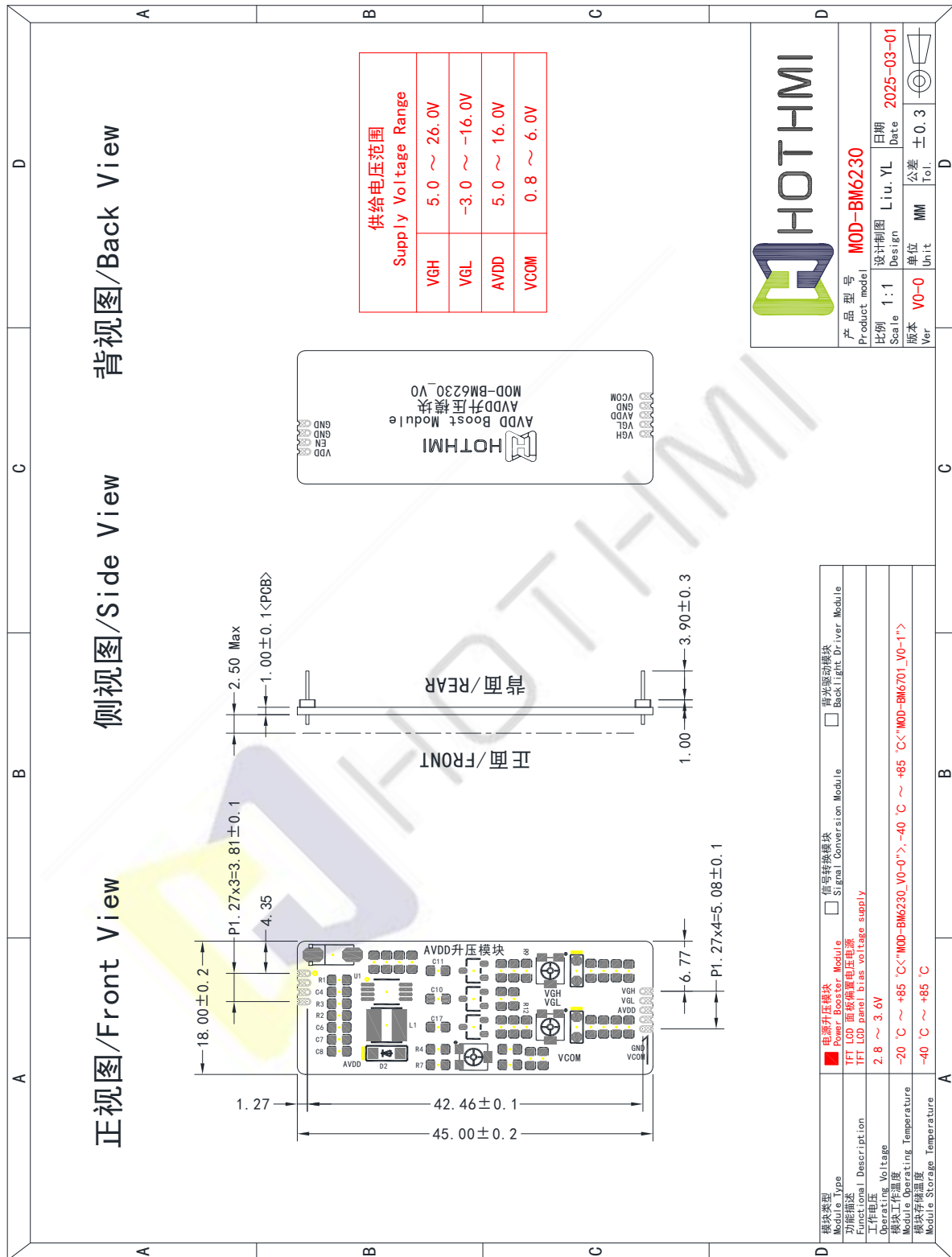
引脚编号 Pin NO.	标号 Symbol	详细描述 Description
1	TP-VDD	电源 Power supply
2	TP-INT	中断信号 Interrupt signal
3	GND	电源地 Power supply ground
4	TP-SDA	IIC数据信号 IIC data signal
5	TP-SCL	IIC时钟信号 IIC clock signal
6	TP-RTN	系统复位 System reset
- 结束 - - END -		



背光模块尺寸 Backlight Module Dimensions

说明 1: 我司所有背光模块长, 宽尺寸相同, 引脚定义相同。使用的模块以实物为准。

Note 1: All of our backlight modules have the same length and width dimensions and the same pin definition. Modules used are subject to physical.



AVDD 升压模块尺寸

AVDD Boost Module Dimensions

文档修订记录
Document revision history

版本 Version	日期 DATE	修改说明 Modify description	编著 Editorial
0-0	2026-04-02	初次编制 First compilation.	Liu. YL

-- 结束 --
-- END --