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ST7512 Data Sheet

TFT Single Chip Driver

For 240 x 320 dots, α -Si TFT LCD, 16 Gray Scales

With MCU Interface

Version 2.0

June 2021

Hazardous Substance Free

RoHS/ REACH Compliant

AEC-Q100 Compliant for Automotive Applications

Forcelead Technology Corporation



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1. INTRODUCTION

The ST7512 is a 1-chip driver for driving amorphous Si-TFT with built-in data RAM that contains 240 x 320 dots, supporting 16-, 4-, and 2-gray scale display. It includes built-in power supply circuit that all voltage level are generated for display, and it can be directly connected to MPU bus with 8bit parallel interface or 4-wire serial interface. ST7512 can drive the LCD panel without external clock, so that it is possible to make a display system with the fewest components and minimal power consumption.

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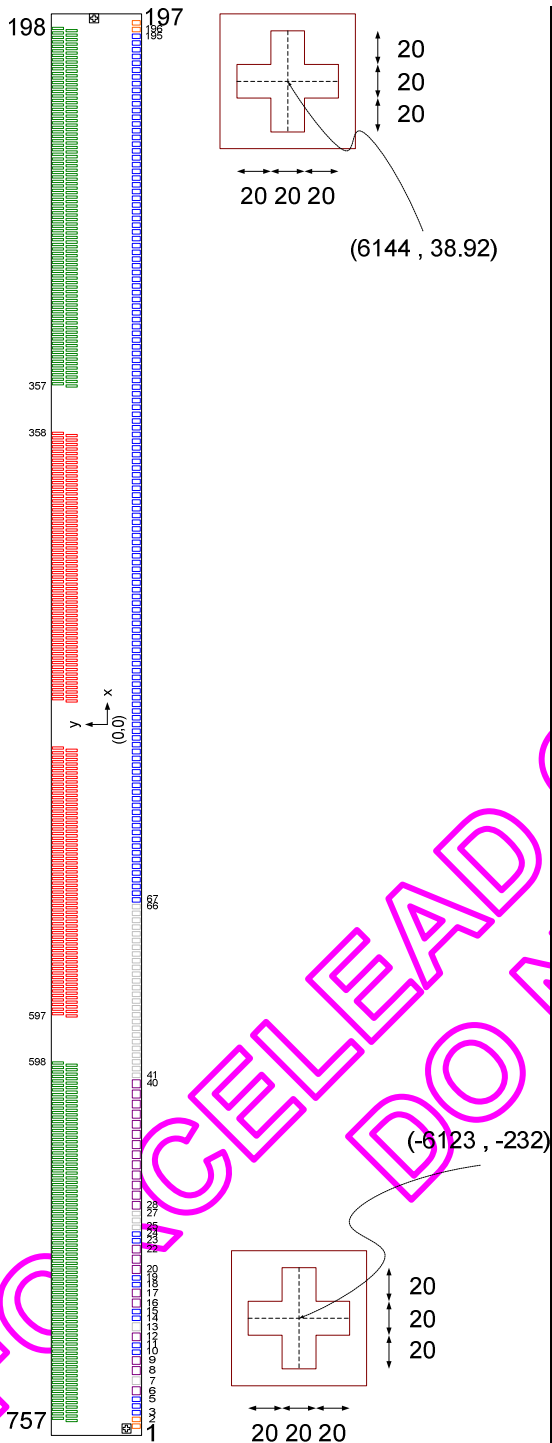
2. FEATURES

- **Single-chip Mono-color TFT-LCD Controller & Driver**
- **Gray Scale**
 - 16 Gray scale (4BPP)
 - 4 Gray scale (2BPP)
 - 2 Gray scale (1BPP)
- **Display RAM**
 - Capacity: $240 \times 320 \times 4 = 307,200$ bits
 - ◆ 1BPP mode: 4 data frame are available.
 - ◆ 2BPP mode: 2 data frame are available.
 - ◆ 4BPP mode and 160 lines or less: 2 data frame are available
- **Interface**
 - 8-bit parallel bi-directional interface with 6800 and 8080
 - 4-line SPI
 - 3-line SPI
- **DC-VCOM Driving Methods**
 - Dot inversion
- **Temperature Compensation Functions**
 - Voltage
 - ◆ GVDD and GVCL temperature compensation
 - ◆ VCOM temperature compensation
 - ◆ VGH temperature compensation
 - Frame rate temperature compensation
- **Operation Voltage**
 - Input voltage:
 - ◆ Analog power supply: 3.0V ~ 5.0V
 - ◆ IO power supply: 3.0V ~ 5.0V
 - Output voltage:
 - ◆ Max. gate voltage: $V_{GH} - V_{GL} = 30V$
 - ◆ Max. source voltage: $GVDD = 5.8V$
 - ◆ VCOM voltage: 0V ~ -2V
- **None Volatility Memory**
 - MTP
 - ◆ VCOM offset: 8bit x 2
 - ◆ User ID: 8bit x 2
- **Cyclic redundancy check (CRC)**
- **Temperature Range: -40°C ~ 105°C**
- **Package Type: COG**



3. PACKAGE INFORMATION

3.1 ST7512 COG Outline (Gold Bump Face-up)



Item	Dimension(um)	
Chip length (x)	12,414	
Chip width (y)	756	
Chip thickness	300	
Bump height	15	
Linear coefficient (α) of thermal expansion($10^{-6}/^{\circ}\text{C}$)		
2.6		
Type A		
Pin	198~757	
	Item	Dimension(um)
	A1	22
	A2	100
	A3	18
	A4	40
	A5	20
A6	20	
Type B		
Pin	1~5, 10~11, 14~15, 18~19, 23~24, 67~197	
	Item	Dimension(um)
	B1	40
	B2	70
	B3	20
B4	60	
Type C		
Pin	41~66	
	Item	Dimension(um)
	C1	32
	C2	70
	C3	18
C4	50	
Type D		
Pin	6~9, 12~13, 16~17, 20~22, 28~40	
	Item	Dimension(um)
	D1	70
	D2	70
	D3	20
D4	90	



3.2 Pad Center Coordinates

Pad	Name	X	Y
1	BumpTestL	-6105	-312
2	BumpTestL	-6045	-312
3	VPP	-5990	-312
4	VPP	-5930	-312
5	VPP	-5870	-312
6	EXTB	-5795	-312
7	TPSYNC	-5705	-312
8	VSYNCO	-5615	-312
9	CLP	-5525	-312
10	VDDI	-5450	-312
11	VDDI	-5390	-312
12	RSTEN	-5315	-312
13	TCEN	-5225	-312
14	DGND	-5150	-312
15	DGND	-5090	-312
16	PX2SET	-5015	-312
17	EXAVDD	-4925	-312
18	VDDI	-4850	-312
19	VDDI	-4790	-312
20	IF0	-4715	-312
21	IF1	-4625	-312
22	CLS	-4535	-312
23	DGND	-4465	-312
24	DGND	-4405	-312
25	Dummy	-4345	-312
26	Dummy	-4285	-312
27	Dummy	-4225	-312
28	RSTB	-4155	-312
29	CSB	-4065	-312
30	A0	-3975	-312
31	RWR	-3885	-312
32	ERD	-3795	-312
33	D0	-3705	-312
34	D1	-3615	-312
35	D2	-3525	-312
36	D3	-3435	-312
37	D4	-3345	-312
38	D5	-3255	-312
39	D6	-3165	-312
40	D7	-3075	-312
41	T1	-3005	-312
42	T2	-2955	-312

Pad	Name	X	Y
43	T3	-2905	-312
44	T4	-2855	-312
45	TFCOM0	-2805	-312
46	T5	-2755	-312
47	T6	-2705	-312
48	T7	-2655	-312
49	T8	-2605	-312
50	T9	-2555	-312
51	T10	-2505	-312
52	T11	-2455	-312
53	T12	-2405	-312
54	T13	-2355	-312
55	TFCOM1	-2305	-312
56	T14	-2255	-312
57	T15	-2205	-312
58	T16	-2155	-312
59	T17	-2105	-312
60	T18	-2055	-312
61	T19	-2005	-312
62	T20	-1955	-312
63	T21	-1905	-312
64	T22	-1855	-312
65	T23	-1805	-312
66	TFCOM2	-1755	-312
67	VREFC	-1700	-312
68	VREFC	-1640	-312
69	VCCI	-1580	-312
70	VCCI	-1520	-312
71	VCCI	-1460	-312
72	VCCO	-1400	-312
73	VCCO	-1340	-312
74	DGND	-1280	-312
75	DGND	-1220	-312
76	DGND	-1160	-312
77	DGND	-1100	-312
78	DGND	-1040	-312
79	DGND	-980	-312
80	DGND	-920	-312
81	VDDI	-860	-312
82	VDDI	-800	-312
83	VDDI	-740	-312
84	VDDI	-680	-312



Pad	Name	X	Y
85	VDDI	-620	-312
86	VDDI	-560	-312
87	VDDP	-500	-312
88	VDDP	-440	-312
89	PGND	-380	-312
90	PGND	-320	-312
91	AGND	-260	-312
92	AGND	-200	-312
93	VDDA	-140	-312
94	VCOM	-80	-312
95	VCOM	-20	-312
96	VCOM	40	-312
97	VCOM	100	-312
98	GVCL	160	-312
99	GVCL	220	-312
100	GVDD	280	-312
101	GVDD	340	-312
102	VDDA	400	-312
103	VDDA	460	-312
104	VDDA	520	-312
105	VDDA	580	-312
106	VDDA	640	-312
107	VDDA	700	-312
108	C11N	760	-312
109	C11N	820	-312
110	C11N	880	-312
111	C11N	940	-312
112	C11N	1000	-312
113	C11P	1060	-312
114	C11P	1120	-312
115	C11P	1180	-312
116	C11P	1240	-312
117	C11P	1300	-312
118	C12N	1360	-312
119	C12N	1420	-312
120	C12N	1480	-312
121	C12N	1540	-312
122	C12N	1600	-312
123	C12P	1660	-312
124	C12P	1720	-312
125	C12P	1780	-312
126	C12P	1840	-312
127	C12P	1900	-312

Pad	Name	X	Y
128	VDDA	1960	-312
129	AVDD	2020	-312
130	AVDD	2080	-312
131	AVDD	2140	-312
132	AVDD	2200	-312
133	AVDD	2260	-312
134	AGND	2320	-312
135	AGND	2380	-312
136	AGND	2440	-312
137	AGND	2500	-312
138	AGND	2560	-312
139	AGND	2620	-312
140	AGND	2680	-312
141	AGND	2740	-312
142	C21N	2800	-312
143	C21N	2860	-312
144	C21N	2920	-312
145	C21N	2980	-312
146	C21N	3040	-312
147	C21N	3100	-312
148	C21P	3160	-312
149	C21P	3220	-312
150	C21P	3280	-312
151	C21P	3340	-312
152	C21P	3400	-312
153	C21P	3460	-312
154	C22N	3520	-312
155	C22N	3580	-312
156	C22N	3640	-312
157	C22N	3700	-312
158	C22N	3760	-312
159	C22N	3820	-312
160	C22P	3880	-312
161	C22P	3940	-312
162	C22P	4000	-312
163	C22P	4060	-312
164	C22P	4120	-312
165	C22P	4180	-312
166	AVCL	4240	-312
167	AVCL	4300	-312
168	AVCL	4360	-312
169	AVCL	4420	-312
170	AVCL	4480	-312

Pad	Name	X	Y
171	AVCL	4540	-312
172	AGND	4600	-312
173	VGL	4660	-312
174	VGL	4720	-312
175	VGL	4780	-312
176	C33N	4840	-312
177	C33N	4900	-312
178	C33P	4960	-312
179	C33P	5020	-312
180	C32N	5080	-312
181	C32N	5140	-312
182	C32P	5200	-312
183	C32P	5260	-312
184	C31N	5320	-312
185	C31N	5380	-312
186	C31P	5440	-312
187	C31P	5500	-312
188	AGND	5560	-312
189	AGND	5620	-312
190	VGH	5680	-312
191	VGH	5740	-312
192	C41N	5800	-312
193	C41N	5860	-312
194	C41P	5920	-312
195	C41P	5980	-312
196	BumpTestR	6040	-312
197	BumpTestR	6100	-312
198	G2	5942	297
199	G4	5922	177
200	G6	5902	297
201	G8	5882	177
202	G10	5862	297
203	G12	5842	177
204	G14	5822	297
205	G16	5802	177
206	G18	5782	297
207	G20	5762	177
208	G22	5742	297
209	G24	5722	177
210	G26	5702	297
211	G28	5682	177
212	G30	5662	297
213	G32	5642	177

Pad	Name	X	Y
214	G34	5622	297
215	G36	5602	177
216	G38	5582	297
217	G40	5562	177
218	G42	5542	297
219	G44	5522	177
220	G46	5502	297
221	G48	5482	177
222	G50	5462	297
223	G52	5442	177
224	G54	5422	297
225	G56	5402	177
226	G58	5382	297
227	G60	5362	177
228	G62	5342	297
229	G64	5322	177
230	G66	5302	297
231	G68	5282	177
232	G70	5262	297
233	G72	5242	177
234	G74	5222	297
235	G76	5202	177
236	G78	5182	297
237	G80	5162	177
238	G82	5142	297
239	G84	5122	177
240	G86	5102	297
241	G88	5082	177
242	G90	5062	297
243	G92	5042	177
244	G94	5022	297
245	G96	5002	177
246	G98	4982	297
247	G100	4962	177
248	G102	4942	297
249	G104	4922	177
250	G106	4902	297
251	G108	4882	177
252	G110	4862	297
253	G112	4842	177
254	G114	4822	297
255	G116	4802	177
256	G118	4782	297



Pad	Name	X	Y
257	G120	4762	177
258	G122	4742	297
259	G124	4722	177
260	G126	4702	297
261	G128	4682	177
262	G130	4662	297
263	G132	4642	177
264	G134	4622	297
265	G136	4602	177
266	G138	4582	297
267	G140	4562	177
268	G142	4542	297
269	G144	4522	177
270	G146	4502	297
271	G148	4482	177
272	G150	4462	297
273	G152	4442	177
274	G154	4422	297
275	G156	4402	177
276	G158	4382	297
277	G160	4362	177
278	G162	4342	297
279	G164	4322	177
280	G166	4302	297
281	G168	4282	177
282	G170	4262	297
283	G172	4242	177
284	G174	4222	297
285	G176	4202	177
286	G178	4182	297
287	G180	4162	177
288	G182	4142	297
289	G184	4122	177
290	G186	4102	297
291	G188	4082	177
292	G190	4062	297
293	G192	4042	177
294	G194	4022	297
295	G196	4002	177
296	G198	3982	297
297	G200	3962	177
298	G202	3942	297
299	G204	3922	177

Pad	Name	X	Y
300	G206	3902	297
301	G208	3882	177
302	G210	3862	297
303	G212	3842	177
304	G214	3822	297
305	G216	3802	177
306	G218	3782	297
307	G220	3762	177
308	G222	3742	297
309	G224	3722	177
310	G226	3702	297
311	G228	3682	177
312	G230	3662	297
313	G232	3642	177
314	G234	3622	297
315	G236	3602	177
316	G238	3582	297
317	G240	3562	177
318	G242	3542	297
319	G244	3522	177
320	G246	3502	297
321	G248	3482	177
322	G250	3462	297
323	G252	3442	177
324	G254	3422	297
325	G256	3402	177
326	G258	3382	297
327	G260	3362	177
328	G262	3342	297
329	G264	3322	177
330	G266	3302	297
331	G268	3282	177
332	G270	3262	297
333	G272	3242	177
334	G274	3222	297
335	G276	3202	177
336	G278	3182	297
337	G280	3162	177
338	G282	3142	297
339	G284	3122	177
340	G286	3102	297
341	G288	3082	177
342	G290	3062	297



Pad	Name	X	Y
343	G292	3042	177
344	G294	3022	297
345	G296	3002	177
346	G298	2982	297
347	G300	2962	177
348	G302	2942	297
349	G304	2922	177
350	G306	2902	297
351	G308	2882	177
352	G310	2862	297
353	G312	2842	177
354	G314	2822	297
355	G316	2802	177
356	G318	2782	297
357	G320	2762	177
358	S240	2510	297
359	S239	2490	177
360	S238	2470	297
361	S237	2450	177
362	S236	2430	297
363	S235	2410	177
364	S234	2390	297
365	S233	2370	177
366	S232	2350	297
367	S231	2330	177
368	S230	2310	297
369	S229	2290	177
370	S228	2270	297
371	S227	2250	177
372	S226	2230	297
373	S225	2210	177
374	S224	2190	297
375	S223	2170	177
376	S222	2150	297
377	S221	2130	177
378	S220	2110	297
379	S219	2090	177
380	S218	2070	297
381	S217	2050	177
382	S216	2030	297
383	S215	2010	177
384	S214	1990	297
385	S213	1970	177

Pad	Name	X	Y
386	S212	1950	297
387	S211	1930	177
388	S210	1910	297
389	S209	1890	177
390	S208	1870	297
391	S207	1850	177
392	S206	1830	297
393	S205	1810	177
394	S204	1790	297
395	S203	1770	177
396	S202	1750	297
397	S201	1730	177
398	S200	1710	297
399	S199	1690	177
400	S198	1670	297
401	S197	1650	177
402	S196	1630	297
403	S195	1610	177
404	S194	1590	297
405	S193	1570	177
406	S192	1550	297
407	S191	1530	177
408	S190	1510	297
409	S189	1490	177
410	S188	1470	297
411	S187	1450	177
412	S186	1430	297
413	S185	1410	177
414	S184	1390	297
415	S183	1370	177
416	S182	1350	297
417	S181	1330	177
418	S180	1310	297
419	S179	1290	177
420	S178	1270	297
421	S177	1250	177
422	S176	1230	297
423	S175	1210	177
424	S174	1190	297
425	S173	1170	177
426	S172	1150	297
427	S171	1130	177
428	S170	1110	297



Pad	Name	X	Y
429	S169	1090	177
430	S168	1070	297
431	S167	1050	177
432	S166	1030	297
433	S165	1010	177
434	S164	990	297
435	S163	970	177
436	S162	950	297
437	S161	930	177
438	S160	910	297
439	S159	890	177
440	S158	870	297
441	S157	850	177
442	S156	830	297
443	S155	810	177
444	S154	790	297
445	S153	770	177
446	S152	750	297
447	S151	730	177
448	S150	710	297
449	S149	690	177
450	S148	670	297
451	S147	650	177
452	S146	630	297
453	S145	610	177
454	S144	590	297
455	S143	570	177
456	S142	550	297
457	S141	530	177
458	S140	510	297
459	S139	490	177
460	S138	470	297
461	S137	450	177
462	S136	430	297
463	S135	410	177
464	S134	390	297
465	S133	370	177
466	S132	350	297
467	S131	330	177
468	S130	310	297
469	S129	290	177
470	S128	270	297
471	S127	250	177

Pad	Name	X	Y
472	S126	230	297
473	S125	210	177
474	S124	190	297
475	S123	170	177
476	S122	150	297
477	S121	130	177
478	S120	-130	297
479	S119	-150	177
480	S118	-170	297
481	S117	-190	177
482	S116	-210	297
483	S115	-230	177
484	S114	-250	297
485	S113	-270	177
486	S112	-290	297
487	S111	-310	177
488	S110	-330	297
489	S109	-350	177
490	S108	-370	297
491	S107	-390	177
492	S106	-410	297
493	S105	-430	177
494	S104	-450	297
495	S103	-470	177
496	S102	-490	297
497	S101	-510	177
498	S100	-530	297
499	S99	-550	177
500	S98	-570	297
501	S97	-590	177
502	S96	-610	297
503	S95	-630	177
504	S94	-650	297
505	S93	-670	177
506	S92	-690	297
507	S91	-710	177
508	S90	-730	297
509	S89	-750	177
510	S88	-770	297
511	S87	-790	177
512	S86	-810	297
513	S85	-830	177
514	S84	-850	297

Pad	Name	X	Y	Pad	Name	X	Y
515	S83	-870	177	558	S40	-1730	297
516	S82	-890	297	559	S39	-1750	177
517	S81	-910	177	560	S38	-1770	297
518	S80	-930	297	561	S37	-1790	177
519	S79	-950	177	562	S36	-1810	297
520	S78	-970	297	563	S35	-1830	177
521	S77	-990	177	564	S34	-1850	297
522	S76	-1010	297	565	S33	-1870	177
523	S75	-1030	177	566	S32	-1890	297
524	S74	-1050	297	567	S31	-1910	177
525	S73	-1070	177	568	S30	-1930	297
526	S72	-1090	297	569	S29	-1950	177
527	S71	-1110	177	570	S28	-1970	297
528	S70	-1130	297	571	S27	-1990	177
529	S69	-1150	177	572	S26	-2010	297
530	S68	-1170	297	573	S25	-2030	177
531	S67	-1190	177	574	S24	-2050	297
532	S66	-1210	297	575	S23	-2070	177
533	S65	-1230	177	576	S22	-2090	297
534	S64	-1250	297	577	S21	-2110	177
535	S63	-1270	177	578	S20	-2130	297
536	S62	-1290	297	579	S19	-2150	177
537	S61	-1310	177	580	S18	-2170	297
538	S60	-1330	297	581	S17	-2190	177
539	S59	-1350	177	582	S16	-2210	297
540	S58	-1370	297	583	S15	-2230	177
541	S57	-1390	177	584	S14	-2250	297
542	S56	-1410	297	585	S13	-2270	177
543	S55	-1430	177	586	S12	-2290	297
544	S54	-1450	297	587	S11	-2310	177
545	S53	-1470	177	588	S10	-2330	297
546	S52	-1490	297	589	S9	-2350	177
547	S51	-1510	177	590	S8	-2370	297
548	S50	-1530	297	591	S7	-2390	177
549	S49	-1550	177	592	S6	-2410	297
550	S48	-1570	297	593	S5	-2430	177
551	S47	-1590	177	594	S4	-2450	297
552	S46	-1610	297	595	S3	-2470	177
553	S45	-1630	177	596	S2	-2490	297
554	S44	-1650	297	597	S1	-2510	177
555	S43	-1670	177	598	G319	-2762	297
556	S42	-1690	297	599	G317	-2782	177
557	S41	-1710	177	600	G315	-2802	297



Pad	Name	X	Y
601	G313	-2822	177
602	G311	-2842	297
603	G309	-2862	177
604	G307	-2882	297
605	G305	-2902	177
606	G303	-2922	297
607	G301	-2942	177
608	G299	-2962	297
609	G297	-2982	177
610	G295	-3002	297
611	G293	-3022	177
612	G291	-3042	297
613	G289	-3062	177
614	G287	-3082	297
615	G285	-3102	177
616	G283	-3122	297
617	G281	-3142	177
618	G279	-3162	297
619	G277	-3182	177
620	G275	-3202	297
621	G273	-3222	177
622	G271	-3242	297
623	G269	-3262	177
624	G267	-3282	297
625	G265	-3302	177
626	G263	-3322	297
627	G261	-3342	177
628	G259	-3362	297
629	G257	-3382	177
630	G255	-3402	297
631	G253	-3422	177
632	G251	-3442	297
633	G249	-3462	177
634	G247	-3482	297
635	G245	-3502	177
636	G243	-3522	297
637	G241	-3542	177
638	G239	-3562	297
639	G237	-3582	177
640	G235	-3602	297
641	G233	-3622	177
642	G231	-3642	297
643	G229	-3662	177

Pad	Name	X	Y
644	G227	-3682	297
645	G225	-3702	177
646	G223	-3722	297
647	G221	-3742	177
648	G219	-3762	297
649	G217	-3782	177
650	G215	-3802	297
651	G213	-3822	177
652	G211	-3842	297
653	G209	-3862	177
654	G207	-3882	297
655	G205	-3902	177
656	G203	-3922	297
657	G201	-3942	177
658	G199	-3962	297
659	G197	-3982	177
660	G195	-4002	297
661	G193	-4022	177
662	G191	-4042	297
663	G189	-4062	177
664	G187	-4082	297
665	G185	-4102	177
666	G183	-4122	297
667	G181	-4142	177
668	G179	-4162	297
669	G177	-4182	177
670	G175	-4202	297
671	G173	-4222	177
672	G171	-4242	297
673	G169	-4262	177
674	G167	-4282	297
675	G165	-4302	177
676	G163	-4322	297
677	G161	-4342	177
678	G159	-4362	297
679	G157	-4382	177
680	G155	-4402	297
681	G153	-4422	177
682	G151	-4442	297
683	G149	-4462	177
684	G147	-4482	297
685	G145	-4502	177
686	G143	-4522	297



Pad	Name	X	Y
687	G141	-4542	177
688	G139	-4562	297
689	G137	-4582	177
690	G135	-4602	297
691	G133	-4622	177
692	G131	-4642	297
693	G129	-4662	177
694	G127	-4682	297
695	G125	-4702	177
696	G123	-4722	297
697	G121	-4742	177
698	G119	-4762	297
699	G117	-4782	177
700	G115	-4802	297
701	G113	-4822	177
702	G111	-4842	297
703	G109	-4862	177
704	G107	-4882	297
705	G105	-4902	177
706	G103	-4922	297
707	G101	-4942	177
708	G99	-4962	297
709	G97	-4982	177
710	G95	-5002	297
711	G93	-5022	177
712	G91	-5042	297
713	G89	-5062	177
714	G87	-5082	297
715	G85	-5102	177
716	G83	-5122	297
717	G81	-5142	177
718	G79	-5162	297
719	G77	-5182	177
720	G75	-5202	297
721	G73	-5222	177
722	G71	-5242	297

Pad	Name	X	Y
723	G69	-5262	177
724	G67	-5282	297
725	G65	-5302	177
726	G63	-5322	297
727	G61	-5342	177
728	G59	-5362	297
729	G57	-5382	177
730	G55	-5402	297
731	G53	-5422	177
732	G51	-5442	297
733	G49	-5462	177
734	G47	-5482	297
735	G45	-5502	177
736	G43	-5522	297
737	G41	-5542	177
738	G39	-5562	297
739	G37	-5582	177
740	G35	-5602	297
741	G33	-5622	177
742	G31	-5642	297
743	G29	-5662	177
744	G27	-5682	297
745	G25	-5702	177
746	G23	-5722	297
747	G21	-5742	177
748	G19	-5762	297
749	G17	-5782	177
750	G15	-5802	297
751	G13	-5822	177
752	G11	-5842	297
753	G9	-5862	177
754	G7	-5882	297
755	G5	-5902	177
756	G3	-5922	297
757	G1	-5942	177



3.3 Ordering Information

Part Number	Package
ST7512-Gx	G : COG x = 5: chip thickness 250um 6: chip thickness 200um

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4. BLOCK DIAGRAM

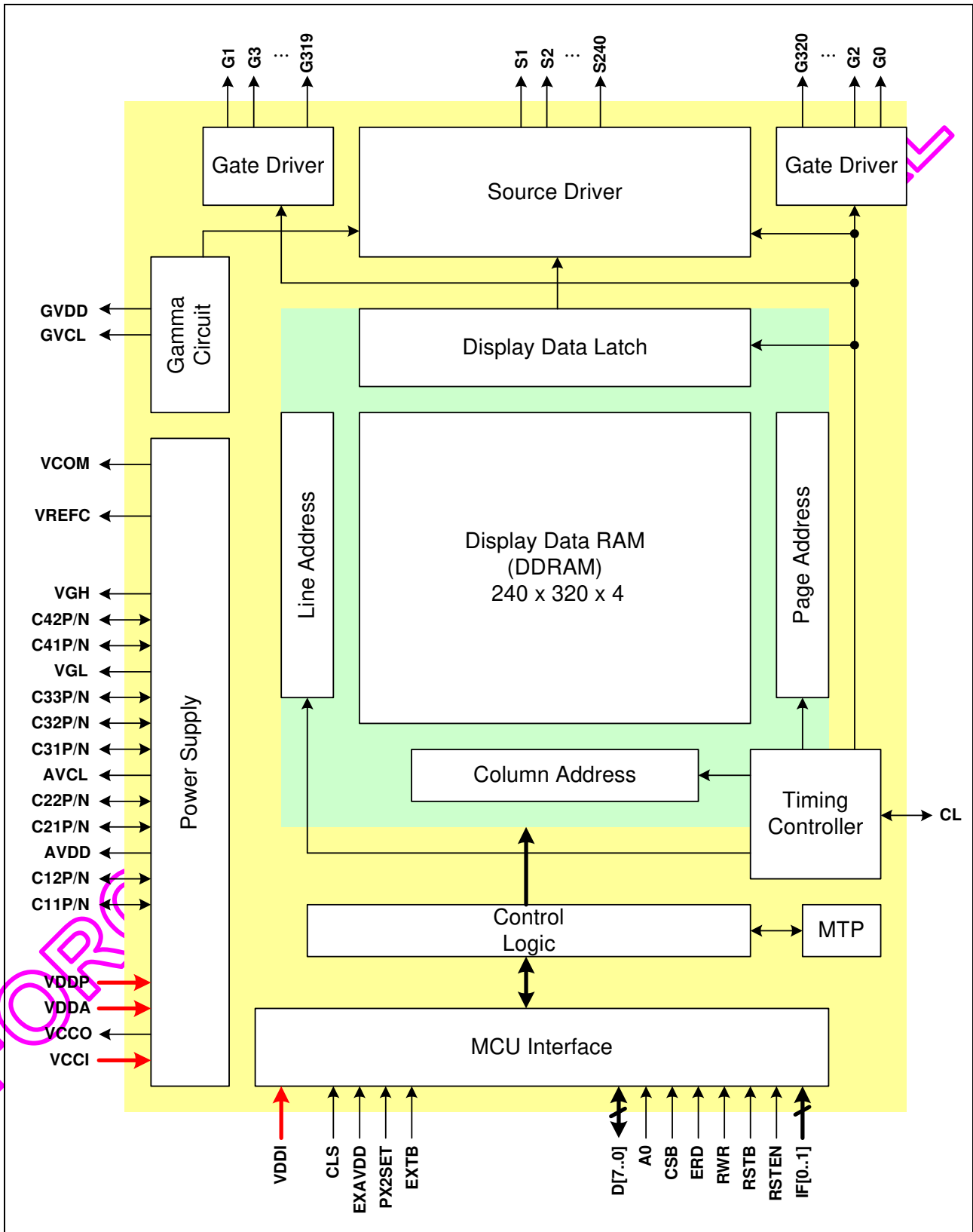


Fig. 1 Block Diagram



5. PIN DESCRIPTION

5.1 Microprocessor Interface Pins

Pin Name	Type	Description															
IF[1:0]	I	IF1 selects the interface mode (Serial or Parallel), and IF0 selects the microprocessor type in parallel interface mode (8080-series or 6800-series).															
		<table border="1"> <thead> <tr> <th>IF1</th> <th>IF0</th> <th>Selected Interface</th> </tr> </thead> <tbody> <tr> <td>L</td> <td>L</td> <td>8-bit 8080 parallel interface</td> </tr> <tr> <td>L</td> <td>H</td> <td>8-bit 6800 parallel interface</td> </tr> <tr> <td>H</td> <td>L</td> <td>3-line serial interface</td> </tr> <tr> <td>H</td> <td>H</td> <td>4-line serial interface</td> </tr> </tbody> </table>	IF1	IF0	Selected Interface	L	L	8-bit 8080 parallel interface	L	H	8-bit 6800 parallel interface	H	L	3-line serial interface	H	H	4-line serial interface
		IF1	IF0	Selected Interface													
		L	L	8-bit 8080 parallel interface													
		L	H	8-bit 6800 parallel interface													
H	L	3-line serial interface															
H	H	4-line serial interface															
RSTB	I	Reset input pin. Active when it is low. This pin is effective when RSTEN pin is "H". Initialization is executed when this pin is set to "L". SWRESET command must be required after initialization.															
RSTEN	I	Distinction pin of the RSTB pin signal. RESEN="H": RSTB pin is effective. RESEN="L": RSTB pin is not effective.															
CSB	I	Chip select input pin. Interface access is enabled when CSB is "L" in parallel, SPI interface. When CSB is non-active (CSB="H"), D[7:0] pins are high impedance.															
A0	I	Data/Command identification pin. A0="H": Display data or parameter A0="L": Command When using 3-line serial interface: A0="H"															
D[7:0]	I/O	When using 8-bit parallel interface. (6800 or 8080 mode) 8-bit bi-directional data bus. Connect to the data bus of 8-bit microprocessor. When chip select pins are not active (CSB="H"), D[7:0] pins are high impedance.															
	I/O	When using serial interface: 3-line or 4-line D7: Serial input clock (SCL). D0: Serial data (SDA). D[6:1]: fix to "H" by VDDI. When chip select pin (CSB) is not active, D[7:0] are high impedance.															
ERD	I	Read/Write execution control pin. When IF1 is "L",															
		<table border="1"> <thead> <tr> <th>IF0</th> <th>MPU Type</th> <th>ERD</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>6800 series</td> <td>E</td> <td>Read/Write control input pin. R/W="H": When E is "H", D[7:0] are in output mode. R/W="L": Signals on D[7:0] are latched at the falling edge of E signal.</td> </tr> <tr> <td>L</td> <td>8080 series</td> <td>/RD</td> <td>Read enable input pin. When /RD is "L", D[7:0] are in output mode.</td> </tr> </tbody> </table>	IF0	MPU Type	ERD	Description	H	6800 series	E	Read/Write control input pin. R/W="H": When E is "H", D[7:0] are in output mode. R/W="L": Signals on D[7:0] are latched at the falling edge of E signal.	L	8080 series	/RD	Read enable input pin. When /RD is "L", D[7:0] are in output mode.			
		IF0	MPU Type	ERD	Description												
H	6800 series	E	Read/Write control input pin. R/W="H": When E is "H", D[7:0] are in output mode. R/W="L": Signals on D[7:0] are latched at the falling edge of E signal.														
L	8080 series	/RD	Read enable input pin. When /RD is "L", D[7:0] are in output mode.														
ERD is not used in serial interface and should fix to "H" by VDDI.																	



Pin Name	Type	Description												
RWR	I	Read/Write execution control pin. When IF1 is "L",												
		<table border="1"> <thead> <tr> <th>IFO</th> <th>MPU Type</th> <th>RWR</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>6800 series</td> <td>R/W</td> <td>Read/Write control input pin. R/W="H": read. R/W="L": write.</td> </tr> <tr> <td>L</td> <td>8080 series</td> <td>/WR</td> <td>Write enable input pin. Signals on D[7:0] will be latched at the rising edge of /WR signal.</td> </tr> </tbody> </table>	IFO	MPU Type	RWR	Description	H	6800 series	R/W	Read/Write control input pin. R/W="H": read. R/W="L": write.	L	8080 series	/WR	Write enable input pin. Signals on D[7:0] will be latched at the rising edge of /WR signal.
		IFO	MPU Type	RWR	Description									
H	6800 series	R/W	Read/Write control input pin. R/W="H": read. R/W="L": write.											
L	8080 series	/WR	Write enable input pin. Signals on D[7:0] will be latched at the rising edge of /WR signal.											
RWR is not used in serial interface and should fix to "H" by VDDI.														
EXAVDD	I	Select pin of AVDD for external power supply.												
		<table border="1"> <thead> <tr> <th>EXAVDD</th> <th>AVDD power supply</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>External</td> <td>AVDD is connected to external power supply.</td> </tr> <tr> <td>L</td> <td>Internal</td> <td>AVDD is generated by internal power circuit.</td> </tr> </tbody> </table>	EXAVDD	AVDD power supply	Description	H	External	AVDD is connected to external power supply.	L	Internal	AVDD is generated by internal power circuit.			
		EXAVDD	AVDD power supply	Description										
H	External	AVDD is connected to external power supply.												
L	Internal	AVDD is generated by internal power circuit.												
PX2SET	I	Select pin of AVDD pump multiplier.												
		<table border="1"> <thead> <tr> <th>PX2SET</th> <th>AVDD pump multiplier.</th> <th>Description</th> </tr> </thead> <tbody> <tr> <td>H</td> <td>x 2</td> <td>VDDA = 5.0V</td> </tr> <tr> <td>L</td> <td>x 3</td> <td>VDDA = 3.3V</td> </tr> </tbody> </table>	PX2SET	AVDD pump multiplier.	Description	H	x 2	VDDA = 5.0V	L	x 3	VDDA = 3.3V			
		PX2SET	AVDD pump multiplier.	Description										
H	x 2	VDDA = 5.0V												
L	x 3	VDDA = 3.3V												
TPSYNCP	O	PWM output pin												
VSYNCO	O	Vertical synchronization signal output pin.												
EXTB	I	For MTP enable pin. (Internal pull-up)												

Note:

- After VDDI is turned ON, any MPU interface pins cannot be left floating.

5.2 LCD Driver Related Pins

Pin Name	Type	Description
S[240:1]	O	TFT-LCD Source Driver Outputs.
G[320:1]	O	TFT-LCD Gate Driver Outputs.

5.3 Clock System Pins

Pin Name	Type	Description
CLS	I	Clock source selection pin. CLS="H": enable internal clock. CLS="L": disable internal clock and use external clock.
CLP	I/O	If CLS="H", internal clock output. If CLS="L", external clock input.

5.4 Power Supply Pins

Pin Name	Type	Description
VDDA	Power	Power supply for analog and booster circuit.
VDDP	Power	Power supply for analog power system.
VDDI	Power	Power supply for IO system.
AGND	Power	System ground for analog and booster circuit.
PGND	Power	System ground for analog power system.
DGND	Power	System ground for IO and digital circuit.
VPP	Power	Power supply for MTP burning.

5.5 LCD Power System Pins

Pin Name	Type	Description
VREFC	O	Monitor pin for internal regulator VREFC
AVDD	Power	Power pin for analog circuits. Connect to a capacitor for stabilization.
AVCL	Power	Power supply pin for generating GVCL. Connect to a capacitor for stabilization.
VGL	O	Power supply pin for gate driver. Connect to a capacitor for stabilization.
VGH	O	Power supply pin for gate driver. Connect to a capacitor for stabilization.
GVDD	O	Power output of positive grayscale voltage generator. When internal GVDD generator is not used, connect an external power supply (AVDD - 0.5V) to this pin.
GVCL	O	Power output of negative grayscale voltage generator. When internal GVCL generator is not used, connect an external power supply (AVCL+0.5V) to this pin.
VCOM	Power	Power supply for the TFT-LCD common electrode.
VCCO	O	Digital reference power voltage output. Connect to a capacitor for stabilization.
VCCI	Power	Digital reference power voltage input
C11P C12P	Power	Flying Capacitor for generating AVDD Output Connecting pins on the positive side. If 1st booster is not used, please open them.
C11N C12N	Power	Flying Capacitor for generating AVDD Output Connecting pins on the negative side. If 1st booster is not used, please open them.
C21P C22P	Power	Flying Capacitor for generating AVCL Output Connecting pins on the positive side. If 2nd booster is not used, please open them.
C21N C22N	Power	Flying Capacitor for generating AVCL Output Connecting pins on the negative side. If 2nd booster is not used, please open them.
C31P C32P C33P	Power	Flying Capacitor for generating VGL Output Connecting pins on the positive side.
C31N C32N C33N	Power	Flying Capacitor for generating VGL Output Connecting pins on the negative side.
C41P	Power	Flying Capacitor for generating VGH Output
C41N	Power	Flying Capacitor for generating VGH Output



5.6 Test Pins

Pin Name	Type	Description
T[23:0]	Open	Reserved for testing only. Leave these pins open.
TFCOM[2:0]	Open	Reserved for testing only. Leave these pins open.
TCEN	GND	Reserved for testing only. Connect to ground.
BUMP_TESTL	Open	Reserved for testing only. Leave these pins open.
BUMP_TESTR	Open	Reserved for testing only. Leave these pins open.

5.7 Dummy Pins

Pin Name	Type	Description
Dummy	Open	Dummy pins. Leave these pins open.

5.8 Recommend Resistance

Item	Pin name	Resistance
Powers	VDDA, VDDP, VDDI, AGND, PGND, DGND	< 10 ohm
Boosters	CxxN/P, AVDD, AVCL	< 10 ohm
Regulators	VCOM, GVDD, GVCL, VGL, VGH	< 10 ohm
Logics	D[7:0], CSB, RSTB, A0, RWR, ERD, IF[1:0], EXAVDD, etc.	< 50 ohm
MTP	VPP	< 20 ohm

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6. FUNCTION DESCRIPTION

6.1 Microprocessor Interface

6.1.1 Chip Selection

CSB pin is used for chip selection. ST7512 can communicate with an MCU when CSB is “L”. If CSB is “H”, the inputs of A0, ERD and RWR with any combination will be ignored and D[7:0] are high impedance. In 3-Line and 4-Line serial interfaces, the internal shift register and serial counter are reset when CSB is “H”.

6.1.2 Interface Selection

The interface selection is controlled by IF[1:0] pins. Please refer to the table below:

Table 1

Setting		MCU Type	Interface Pin Function				
IF1	IF0		CSB	A0	RWR	ERD	D[7:0]
L	L	Parallel 8080 series MCU	CSB	A0	/WR	/RD	D[7:0]
L	H	Parallel 6800 series MCU			R/W	E	
H	H	Serial 4-Line series MCU			-	-	
H	L	Serial 3-Line series MCU			-	-	

Note: The un-used pins are marked as “-” and should be connected to “H” by VDDI.

6.1.3 Parallel Interface

When parallel interface is selected, the interface transmission type will be determined by the combination of the control signals. Please refer to the table below:

Table 2

8080 series MCU		6800 series MCU		A0	CSB	Interface Transmission Type
/WR	/RD	R/W	E			
↑	H	L	↓	L	L	Write Command
↑	H	L	↓	H		Write Display Data or Parameter
H	↓	H	↑	H		Read Display Data or Parameter Start
H	↑	H	↓	H		Read Display Data or Parameter Stop

Note:

1. Reading Display Data or Parameter is specified by the instruction before the read operation.
2. When reading Display Data (DDRAM contents), the first output byte is dummy byte.
3. When reading Parameter (temperature, status and PROM data), the first output byte is valid.

6.1.4 Serial Interface

In serial interface (4-Line or 3-Line), IC is active and the control signals (SDI, SDO, SCL and A0 for 4-Line) are enabled when CSB is “L”. When CSB is “H”, the MCU interface is not active and the internal shift-register and serial-counter are reset.

If CSB is set to “H” before all data bits (8 bits) are entered completely, the data concerned is invalidated. Before entering succeeding sets of data, you must input the data concerned again. In order to avoid transfer error due to incoming noise when writing command or data, it is recommended to set CSB at “H” on byte basis, so that the serial-to-parallel counter and the shift-register can be cleared after each byte of transmission.

6.1.4a 4-Line Serial Interface

In 4-Line serial interface, A0 signal is latched at the 8th rising edge of the SCL signal (refer to 錯誤! 找不到參照來源 · 1).

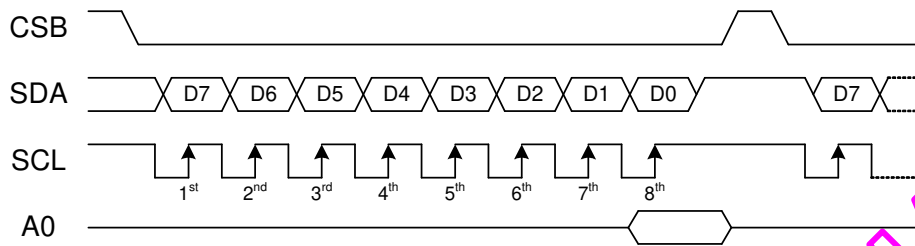


Fig. 2 Write-Operation of 4-Line Serial Interface

After entering the Read Status instruction to read IC status, the information is shifted out as shown below. CSB signal must be kept at “L” during this period. All read out data will be 8 bits.

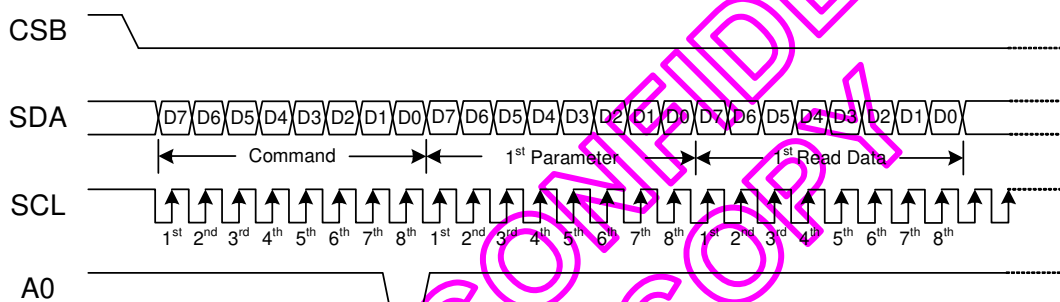


Fig. 3 Read-Operation of 4-Line Serial Interface

6.1.4b 3-Line Serial Interface

In 3-Line interface, A0 signal is not available. The 1st output bit defines command byte or parameter byte (refer to 錯誤! 找不到參照來源 · 3).

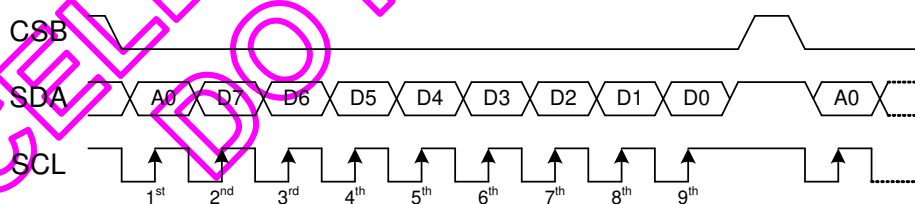


Fig. 4 Write-Operation of 3-Line Serial Interface

After entering the Read Status instruction to read IC status, the information is shifted out as shown below. CSB signal must be kept at “L” during this period. All read out data will be 8 bits.

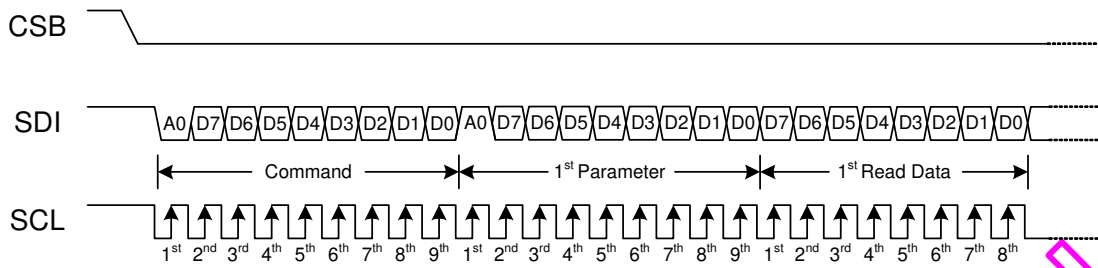


Fig. 5 Read-Operation of 3-Line Serial Interface

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6.1.5 Data Transfer

ST7512 uses bus latch and internal data bus for interface data transfer. When writing data from MPU to the DDRAM, data is automatically transferred from the bus latch to the DDRAM. When reading data from the on-chip DDRAM to MPU, the first read cycle reads the content in bus latch (dummy read) and the data that MPU should read will be output at the next read cycle. That means: after setting the target address, a dummy read cycle is required before the following read-operation. Therefore, the data of the specified address cannot be read at the first read of display data right after setting the address, but can be read at the second read of display data.

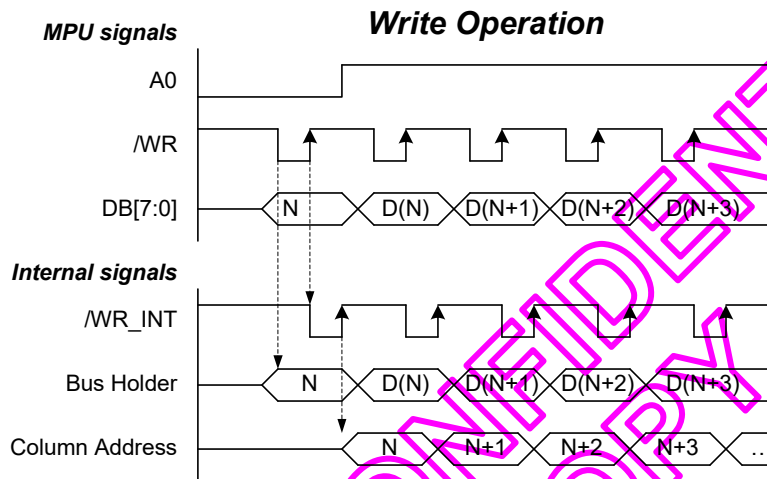


Fig. 6 Data Transfer : Write

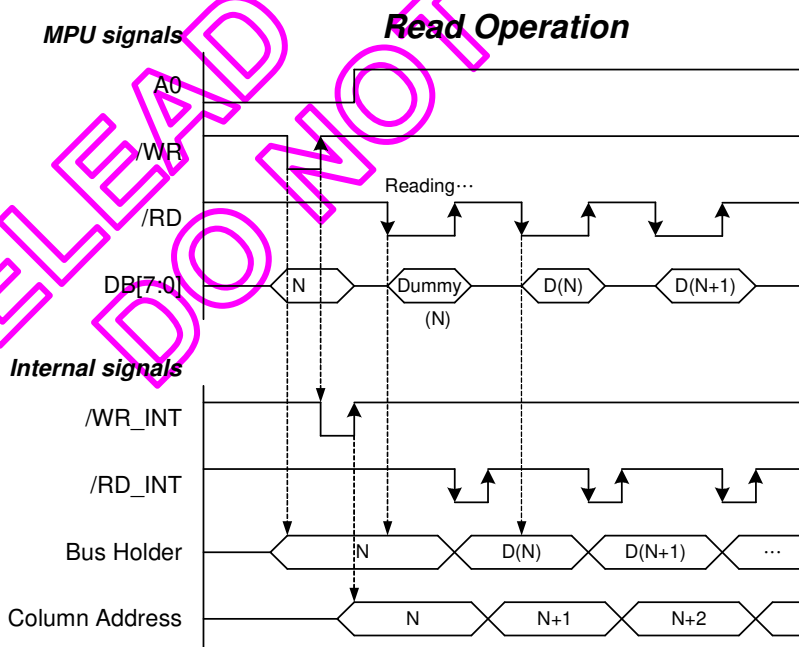


Fig. 7 Data Transfer : Read



6.2 Display Data RAM (DDRAM)

6.2.1 4bpp DDRAM Map

Page address		0	1	2	..	237	238	239	normal	Column address
normal	invert	239	238	237	..	2	1	0	invert	
0	159	D[0:3]	D[0:3]	D[0:3]	..	D[0:3]	D[0:3]	D[0:3]	G1	
		D[4:7]	D[4:7]	D[4:7]	..	D[4:7]	D[4:7]	D[4:7]	G2	
1	158	D[0:3]	D[0:3]	D[0:3]	..	D[0:3]	D[0:3]	D[0:3]	G3	
		D[4:7]	D[4:7]	D[4:7]	..	D[4:7]	D[4:7]	D[4:7]	G4	
:	:	:	:	:	:	:	:	:	:	
158	1	D[0:3]	D[0:3]	D[0:3]	..	D[0:3]	D[0:3]	D[0:3]	G317	
		D[4:7]	D[4:7]	D[4:7]	..	D[4:7]	D[4:7]	D[4:7]	G318	
159	0	D[0:3]	D[0:3]	D[0:3]	..	D[0:3]	D[0:3]	D[0:3]	G319	
		D[4:7]	D[4:7]	D[4:7]	..	D[4:7]	D[4:7]	D[4:7]	G320	
Source		S1	S2	S3	..	S238	S239	S240	Gate	



6.2.2 Mapping of Page, Frame, and Gate

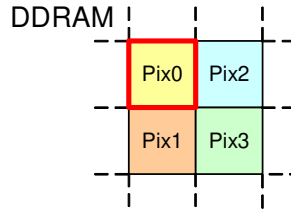
Gate	4bpp mode(>160 lines)		4bpp mode(<=160 lines)		2bpp mode		1bpp mode	
	Page address	Frame address	Page address	Frame address	Page address	Frame address	Page address	Frame address
G1	0	0	0	0/1	0	0/1	0	0/1/2/3
G2			0					
G3	1		1		1			
G4			1					
G5	2		2		2			
G6			2					
G7	3		3		3			
G8			3					
G9	4		4		4			
G10			4					
G311	155	0	75	0/1	77	0/1	38	0/1/2/3
G312			75					
G313	156		76		76			
G314			76					
G315	157		77		77			
G316			77					
G317	158		78		78			
G318			78					
G319	159		79		79			
G320			79					

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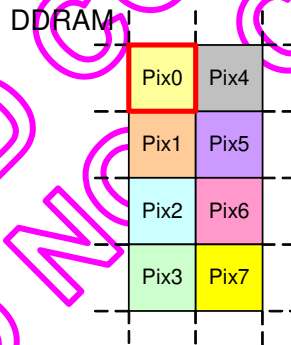


6.2.3 Addressing

4bpp mode	A1	D7	D6	D5	D4	D3	D2	D1	D0
DDRAM write command	0	0	0	1	1	1	0	1	0
	1	1	0	1	0	0	1	0	1
1st write	1	Pix13	Pix12	Pix11	Pix10	Pix03	Pix02	Pix01	Pix00
2nd write	1	Pix33	Pix32	Pix31	Pix30	Pix23	Pix22	Pix21	Pix20

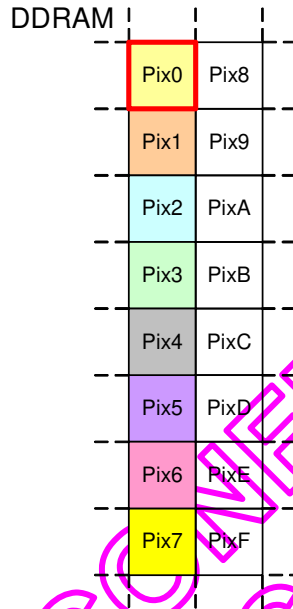


2bpp mode	A1	D7	D6	D5	D4	D3	D2	D1	D0
DDRAM write command	0	0	0	1	1	1	0	1	0
	1	1	0	1	0	0	1	0	1
1st write	1	Pix31	Pix30	Pix21	Pix20	Pix11	Pix10	Pix01	Pix00
2nd write	1	Pix71	Pix70	Pix61	Pix60	Pix51	Pix50	Pix41	Pix40



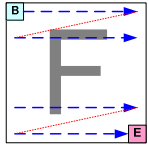
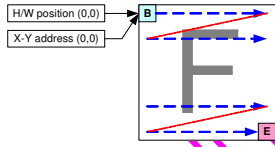
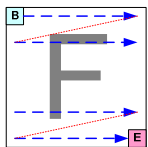
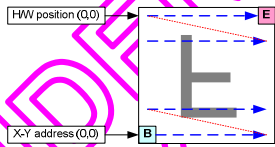
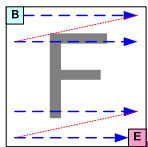
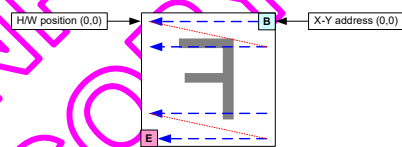
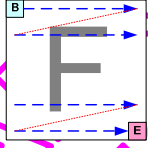
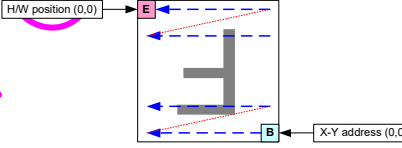
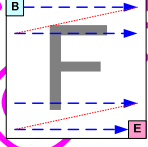
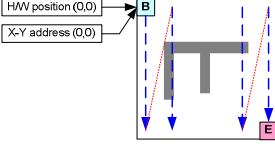
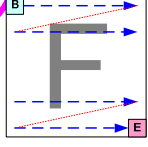
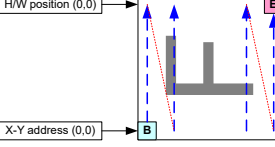
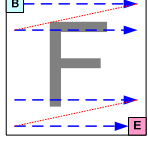
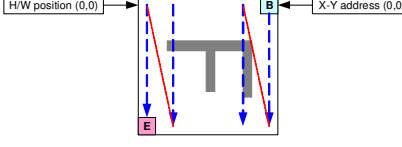


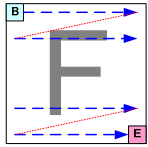
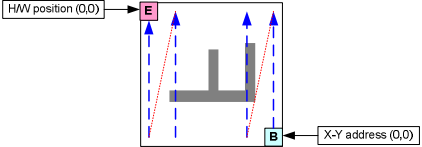
1bpp mode	A1	D7	D6	D5	D4	D3	D2	D1	D0
DDRAM write command	0	0	0	1	1	1	0	1	0
	1	1	0	1	0	0	1	0	1
1st write	1	Pix7	Pix6	Pix5	Pix4	Pix3	Pix2	Pix1	Pix0
2nd write		PixF	PixE	PixD	PixC	PixB	PixA	Pix9	Pix8



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6.2.4 Page Address Circuit and Column Address Circuit

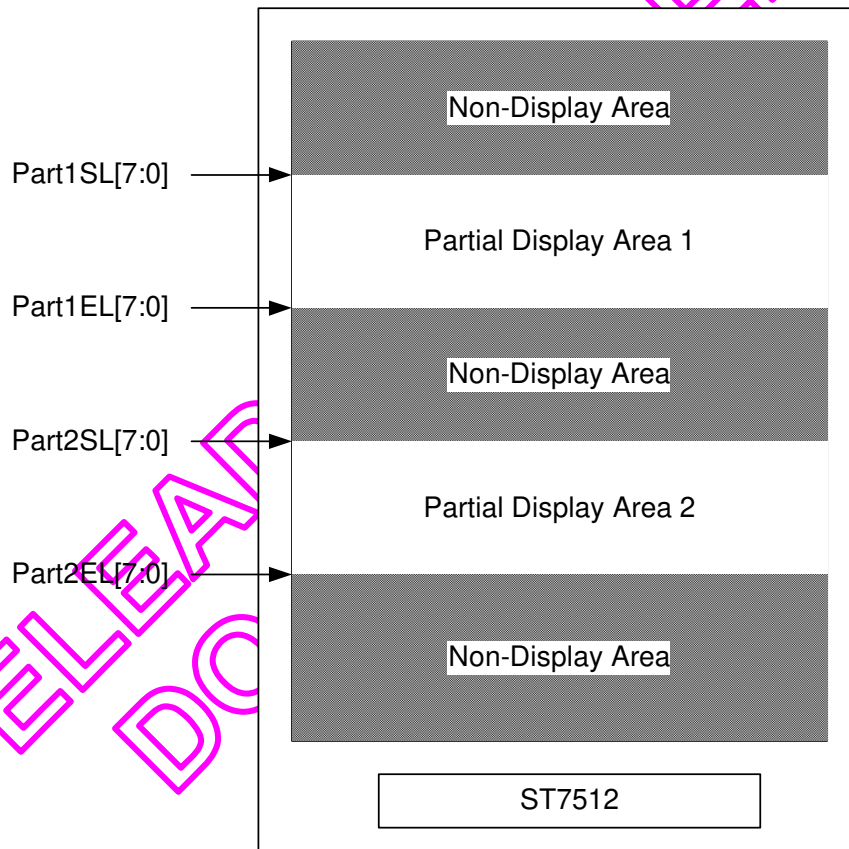
Display data direction	Memory access control			Image in the host	Image in the driver (DDRAM)
	MV	MX	MY		
Normal	0	0	0		
Y-Mirror	0	0	1		
X-Mirror	0	1	0		
X-Mirror Y-Mirror	0	1	1		
X-Y Exchange	1	0	0		
X-Y Exchange Y-Mirror	1	0	1		
X-Y Exchange X-Mirror	1	1	0		

X-Y Exchange	1	1	1		
X-Mirror					
Y-Mirror					

Note: The pattern may need to be modified while rotating.

6.2.5 Partial Display

The ST7512 can support two regions of partial display area in an LCD module. For the first partial display area, the start and end lines are set by the command, Part1SL[7:0] and Part1EL[7:0], respectively. The second partial display area is set by the same way with the command, Part2SL[8:0] and Part2EL[7:0]. The partial display function in the ST7512 is activated by the command, PTLIN(AAh). When the application of normal display is required, the ST7512 can escape from the partial display mode by the command, PTLOUT(A9h).



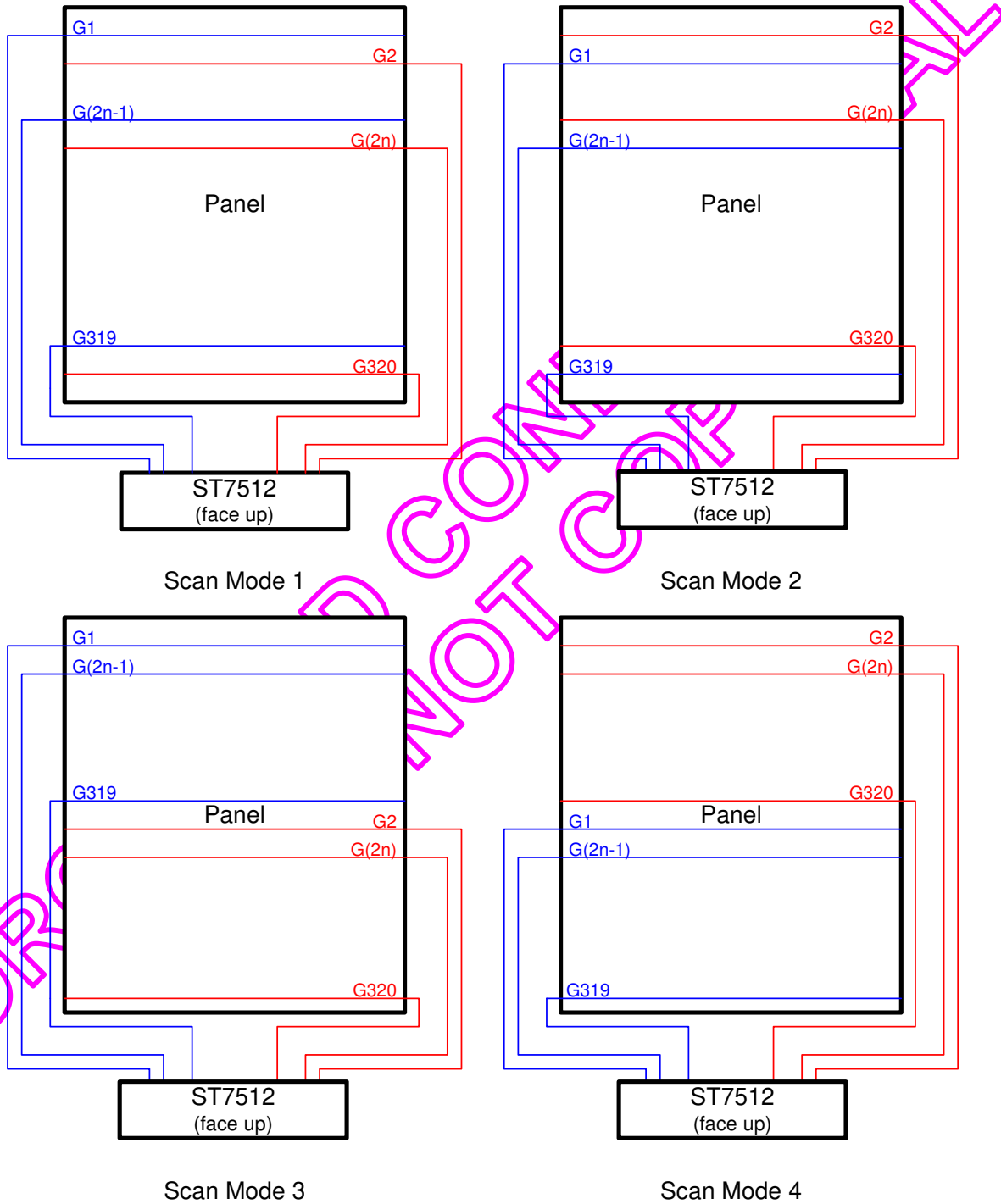


6.3 Oscillation Circuit

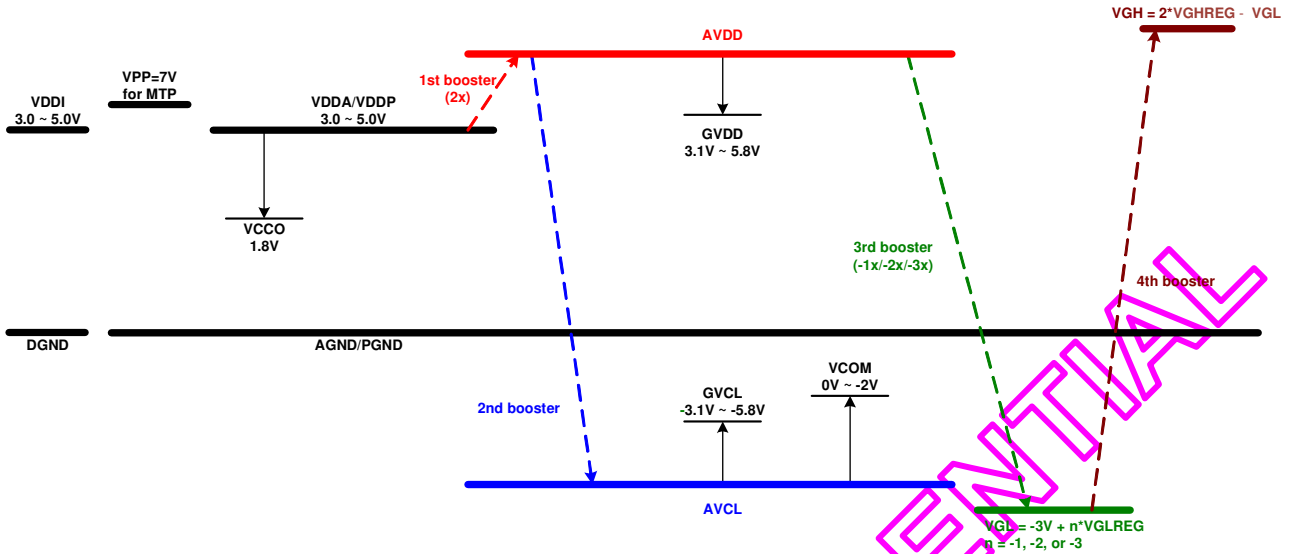
This is on-chip Oscillator without external resistor. When the internal oscillator is used, connect CLS to VDDI; when the external oscillator is used, connect CLS to VSS and input external clock to CLP pin. This oscillator signal is used by the voltage booster and display timing generation circuit.

6.4 Setting Gate Line Scan Mode

ST7512 can support 4 kinds of scan mode.

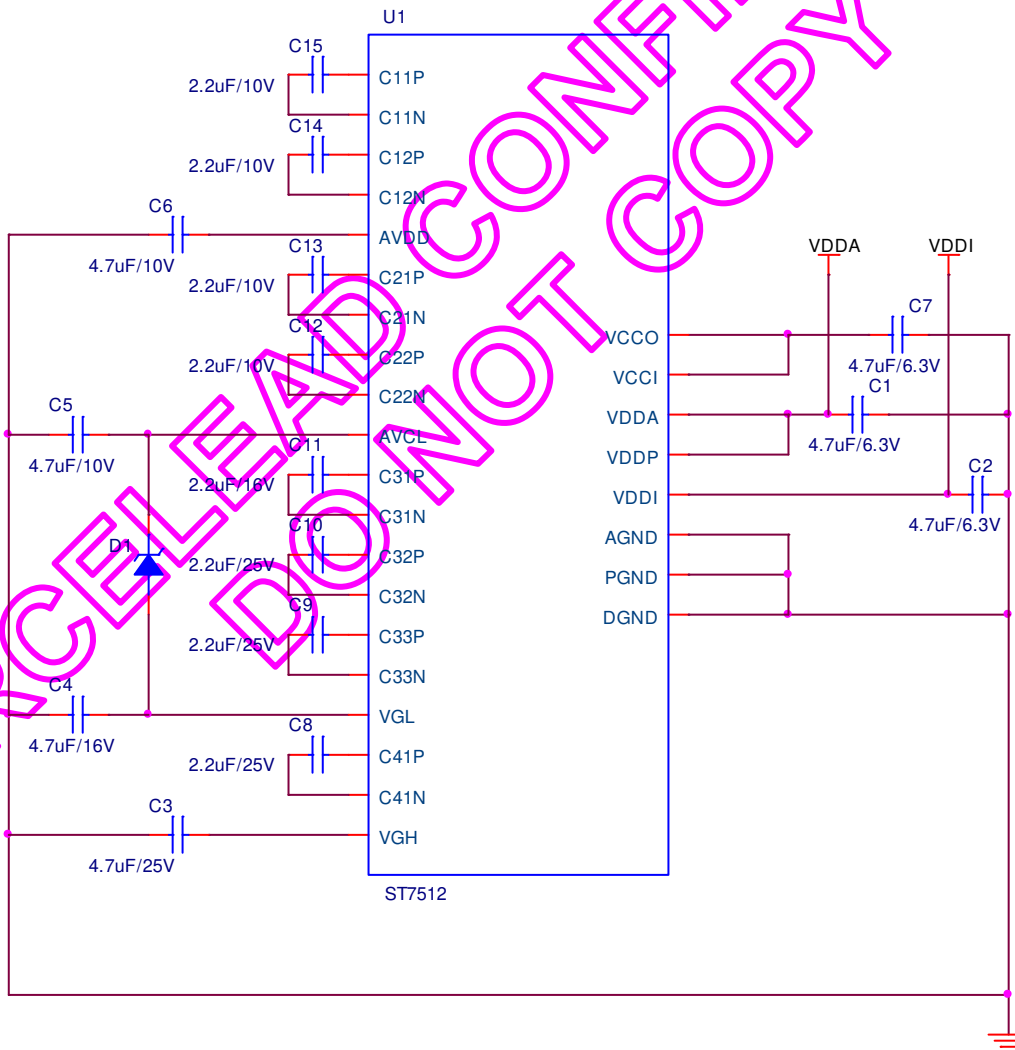


6.5 Power System



6.6 Connection Diagram of External Components

6.6.1 Power Connection of Capacitors





6.6.2 Requirement of External Capacitors

Item	Capacitance (uF)	Rated voltage (V)	Remarks
C1,C2	4.7	6.3	X7R
C3	4.7	25	X7R
C4	4.7	16	X7R
C5,C6	4.7	10	X7R
C7	1 ~ 4.7	6.3	X7R
C8,C9,C10	2.2	25	X7R
C11	2.2	16	X7R
C12,C13,C14,C15	2.2	10	X7R
Item	VF	VR	Remarks
D1	VF < 0.5V/200mA	VR ≥ 25V	SBD

Suggestions of the capacitance are based on the general assumption of 4" panel. Please evaluate the real loading of panels before modifying the value of capacitance.

6.7 Gamma Circuit

This gamma circuit determines 64-level x 2-polarity voltages for grayscale.

For 4bpp mode, these gray levels can be determined by GAMSET4P1~GAMSET4P4 or GAMSET4N1~GAMSET4N4.

For 2bpp mode, these gray levels can be determined by GAMSET2P or GAMSET2N.

For 1bpp mode, these gray levels can be determined by GAMSET1.

GxBPVy[5:0] x = 1 ~ 4, y = 0 ~ F	Equation of voltages	GxBPVy[5:0] x = 1 ~ 4, y = 0 ~ F	Equation of voltages
000000	AGND	100000	GVDD x 32R/63R
000001	GVDD x 1R/63R	100001	GVDD x 33R/63R
000010	GVDD x 2R/63R	100010	GVDD x 34R/63R
000011	GVDD x 3R/63R	100011	GVDD x 35R/63R
000100	GVDD x 4R/63R	100100	GVDD x 36R/63R
000101	GVDD x 5R/63R	100101	GVDD x 37R/63R
000110	GVDD x 6R/63R	100110	GVDD x 38R/63R
000111	GVDD x 7R/63R	100111	GVDD x 39R/63R
001000	GVDD x 8R/63R	101000	GVDD x 40R/63R
001001	GVDD x 9R/63R	101001	GVDD x 41R/63R
001010	GVDD x 10R/63R	101010	GVDD x 42R/63R
001011	GVDD x 11R/63R	101011	GVDD x 43R/63R
001100	GVDD x 12R/63R	101100	GVDD x 44R/63R
001101	GVDD x 13R/63R	101101	GVDD x 45R/63R
001110	GVDD x 14R/63R	101110	GVDD x 46R/63R
001111	GVDD x 15R/63R	101111	GVDD x 47R/63R
010000	GVDD x 16R/63R	110000	GVDD x 48R/63R
010001	GVDD x 17R/63R	110001	GVDD x 49R/63R
010010	GVDD x 18R/63R	110010	GVDD x 50R/63R
010011	GVDD x 19R/63R	110011	GVDD x 51R/63R
010100	GVDD x 20R/63R	110100	GVDD x 52R/63R



GxBPVy[5:0] x = 1 ~ 4, y = 0 ~ F	Equation of voltages	GxBPVy[5:0] x = 1 ~ 4, y = 0 ~ F	Equation of voltages
010101	GVDD x 21R/63R	110101	GVDD x 53R/63R
010110	GVDD x 22R/63R	110110	GVDD x 54R/63R
010111	GVDD x 23R/63R	110111	GVDD x 55R/63R
011000	GVDD x 24R/63R	111000	GVDD x 56R/63R
011001	GVDD x 25R/63R	111001	GVDD x 57R/63R
011010	GVDD x 26R/63R	111010	GVDD x 58R/63R
011011	GVDD x 27R/63R	111011	GVDD x 59R/63R
011100	GVDD x 28R/63R	111100	GVDD x 60R/63R
011101	GVDD x 29R/63R	111101	GVDD x 61R/63R
011110	GVDD x 30R/63R	111110	GVDD x 62R/63R
011111	GVDD x 31R/63R	111111	GVDD

GxBNVy[5:0] x = 1 ~ 4, y = 0 ~ F	Equation of voltages	GxBNVy[5:0] x = 1 ~ 4, y = 0 ~ F	Equation of voltages
000000	AGND	100000	GVCL x 32R/63R
000001	GVCL x 1R/63R	100001	GVCL x 33R/63R
000010	GVCL x 2R/63R	100010	GVCL x 34R/63R
000011	GVCL x 3R/63R	100011	GVCL x 35R/63R
000100	GVCL x 4R/63R	100100	GVCL x 36R/63R
000101	GVCL x 5R/63R	100101	GVCL x 37R/63R
000110	GVCL x 6R/63R	100110	GVCL x 38R/63R
000111	GVCL x 7R/63R	100111	GVCL x 39R/63R
001000	GVCL x 8R/63R	101000	GVCL x 40R/63R
001001	GVCL x 9R/63R	101001	GVCL x 41R/63R
001010	GVCL x 10R/63R	101010	GVCL x 42R/63R
001011	GVCL x 11R/63R	101011	GVCL x 43R/63R
001100	GVCL x 12R/63R	101100	GVCL x 44R/63R
001101	GVCL x 13R/63R	101101	GVCL x 45R/63R
001110	GVCL x 14R/63R	101110	GVCL x 46R/63R
001111	GVCL x 15R/63R	101111	GVCL x 47R/63R
010000	GVCL x 16R/63R	110000	GVCL x 48R/63R
010001	GVCL x 17R/63R	110001	GVCL x 49R/63R
010010	GVCL x 18R/63R	110010	GVCL x 50R/63R
010011	GVCL x 19R/63R	110011	GVCL x 51R/63R
010100	GVCL x 20R/63R	110100	GVCL x 52R/63R
010101	GVCL x 21R/63R	110101	GVCL x 53R/63R
010110	GVCL x 22R/63R	110110	GVCL x 54R/63R
010111	GVCL x 23R/63R	110111	GVCL x 55R/63R
011000	GVCL x 24R/63R	111000	GVCL x 56R/63R
011001	GVCL x 25R/63R	111001	GVCL x 57R/63R
011010	GVCL x 26R/63R	111010	GVCL x 58R/63R
011011	GVCL x 27R/63R	111011	GVCL x 59R/63R



GxBNVy[5:0] x = 1 ~ 4, y = 0 ~ F	Equation of voltages	GxBNVy[5:0] x = 1 ~ 4, y = 0 ~ F	Equation of voltages
011100	GVCL x 28R/63R	111100	GVCL x 60R/63R
011101	GVCL x 29R/63R	111101	GVCL x 61R/63R
011110	GVCL x 30R/63R	111110	GVCL x 62R/63R
011111	GVCL x 31R/63R	111111	GVCL

6.8 Reset

Setting RSTB pin to “L” (hardware reset) can initialize internal function. Generally, VDDI is not stable at the time that the system power is just turned ON. The hardware reset or software reset is required to initialize internal registers after VDDI is stable. Initialization by RSTB pin or command SWRESET is essential before operating.

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6.9 Temperature Compensation Circuit

6.9.1 Set GVDD/GVCL with Temperature Compensation (Temperature ≠ 24°C)

There are 14-line slopes in each temperature step, and customer can select one line slope of temperature compensation coefficient for each temperature step. Each temperature step is 8°C. Please see 錯誤! 找不到參照來源。 as below.

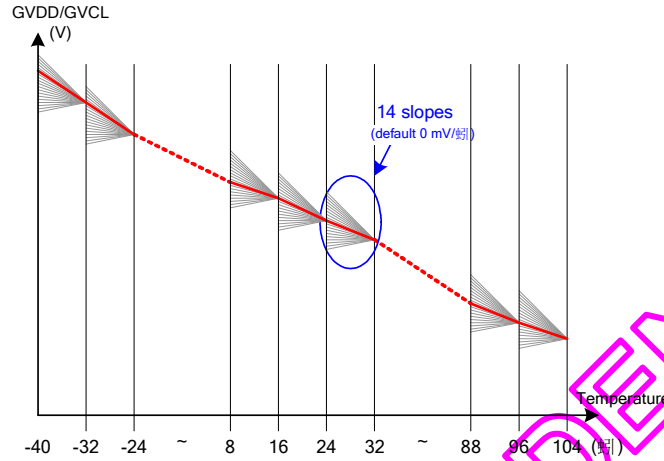


Fig. 8 Temperature Compensation Coefficient Selection

The temperature compensation circuit includes negative and positive temperature gradient slope coefficient. The parameter (MTGVxyy) of Temperature Gradient Set instruction (where x=GV or GC, yy=01, 02, 03,... 11) has a setting value between 0 and 15. MTGVxyy[3]=0 means the sign for the slope of temperature gradient is positive. Otherwise, MTGVxyy[3]=1 means the sign for the slope of temperature gradient is negative. MTGVxyy[2:0] determines the multiplier of the temperature increment by 12.5mV/°C. For example, MTGVxyy[2:0]=1 results the slope of temperature gradient in 1x12.5mV/°C. In other words, if MTGVxyy[3:0]=15, the slope of temperature gradient will be -7x12.5 mV/°C.

Note that each MTGVxyy individually corresponds to a temperature interval; the MTGVxyy means temperature gradient slope coefficient. The relations between MTGVxyy and GVDD/GVCL quantity due to temperature V0(T) are described in the equation shown in Table 3.

Table 3

Temperature Range	Equation GVDD/GVCL(V0) at temperature=T°C
-40°C ≤ T < -32°C	$V_0(T) = V_0(T24) + (-32 - T) \times M_0 + (M_1 + M_2 + M_3 + M_4 + M_5 + M_6 + M_7) \times 8$
-32°C ≤ T < -24°C	$V_0(T) = V_0(T24) + (-24 - T) \times M_1 + (M_2 + M_3 + M_4 + M_5 + M_6 + M_7) \times 8$
-24°C ≤ T < -16°C	$V_0(T) = V_0(T24) + (-16 - T) \times M_2 + (M_3 + M_4 + M_5 + M_6 + M_7) \times 8$
-16°C ≤ T < -8°C	$V_0(T) = V_0(T24) + (-8 - T) \times M_3 + (M_4 + M_5 + M_6 + M_7) \times 8$
-8°C ≤ T < 0°C	$V_0(T) = V_0(T24) + (0 - T) \times M_4 + (M_5 + M_6 + M_7) \times 8$
0°C ≤ T < 8°C	$V_0(T) = V_0(T24) + (8 - T) \times M_5 + (M_6 + M_7) \times 8$
8°C ≤ T < 16°C	$V_0(T) = V_0(T24) + (16 - T) \times M_6 + M_7 \times 8$
16°C ≤ T < 24°C	$V_0(T) = V_0(T24) + (24 - T) \times M_7$
24°C ≤ T < 32°C	$V_0(T) = V_0(T24) - (T - 24) \times M_8$
32°C ≤ T < 40°C	$V_0(T) = V_0(T24) - (T - 32) \times M_9 - M_8 \times 8$
40°C ≤ T < 48°C	$V_0(T) = V_0(T24) - (T - 40) \times M_{A-} - (M_9 + M_8) \times 8$
48°C ≤ T < 56°C	$V_0(T) = V_0(T24) - (T - 48) \times M_B - (M_A + M_9 + M_8) \times 8$
56°C ≤ T < 64°C	$V_0(T) = V_0(T24) - (T - 56) \times M_C - (M_B + M_A + M_9 + M_8) \times 8$



64°C ≤ T < 72°C	$V_0(T) = V_0(T24) - (T - 64) \times MD - (MC + MB + MA + M9 + M8) \times 8$
72°C ≤ T < 80°C	$V_0(T) = V_0(T24) - (T - 72) \times ME - (MD + MC + MB + MA + M9 + M8) \times 8$
80°C ≤ T < 88°C	$V_0(T) = V_0(T24) - (T - 80) \times MF - (ME + MD + MC + MB + MA + M9 + M8) \times 8$
88°C ≤ T < 96°C	$V_0(T) = V_0(T24) - (T - 80) \times M10 - (MF + ME + MD + MC + MB + MA + M9 + M8) \times 8$
96°C ≤ T < 104°C	$V_0(T) = V_0(T24) - (T - 80) \times M11 - (M11 + MF + ME + MD + MC + MB + MA + M9 + M8) \times 8$

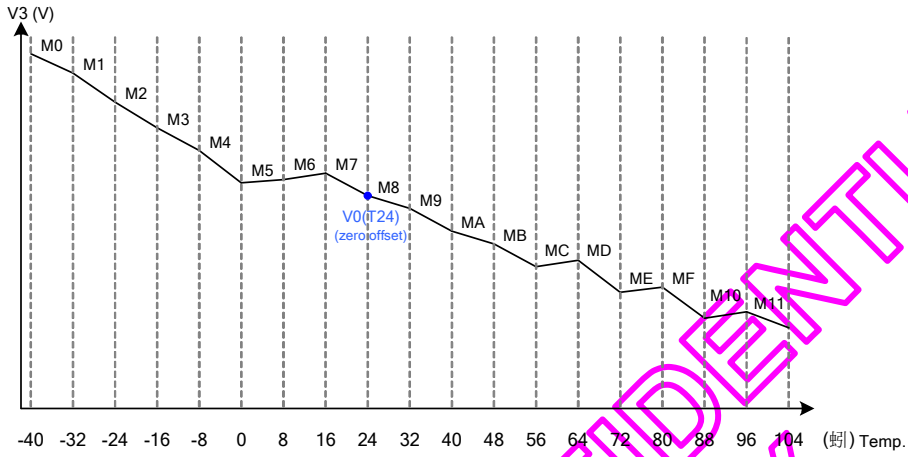


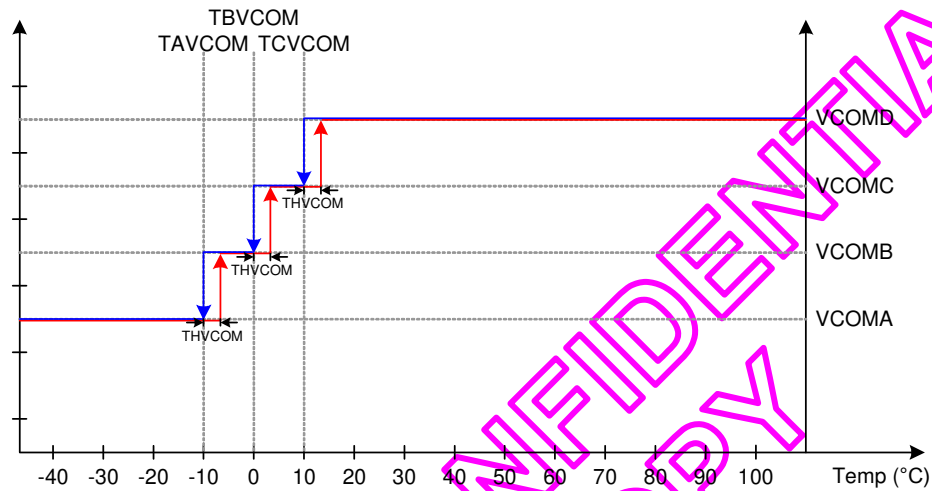
Fig. 9 Temperature Compensation Curve

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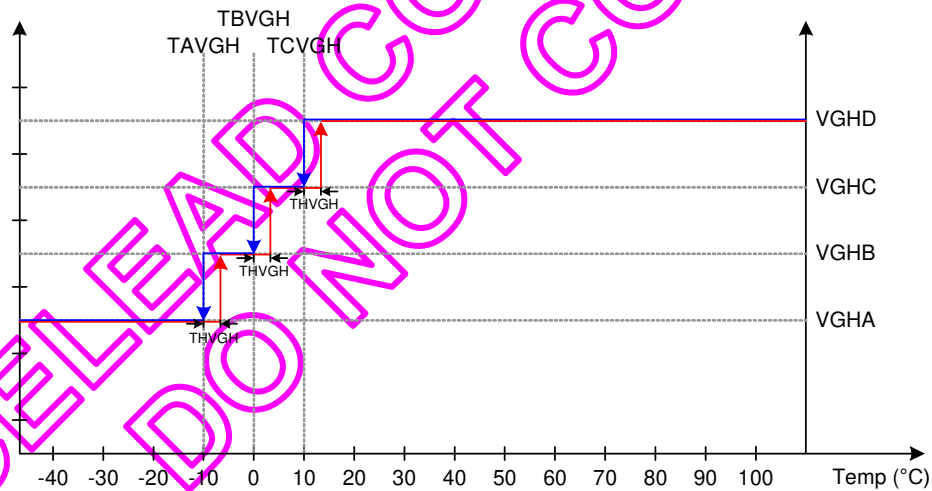


6.9.2 Temperature Gradient Compensation Coefficient of VCOM, VGH, and Frame Rate

ST7512 will auto-switch VCOM in different temperature, such as Fig. 9(a). TA, TB and TC are VCOM switching temperature which can be defined by customer with instruction (C8h). VCOMA, VCOMB, VCOMC and VCOMD are switched VCOM, which also can be defined by customer with instruction (B1h). The temperature hysteresis "THVCOM" in the Fig.9(a) that defines the sensitivity of internal temperature sensor and the value can be altered by instruction. The settings of temperature compensation about VGH and frame rate are in the same way with VCOM.



(a)



(b)

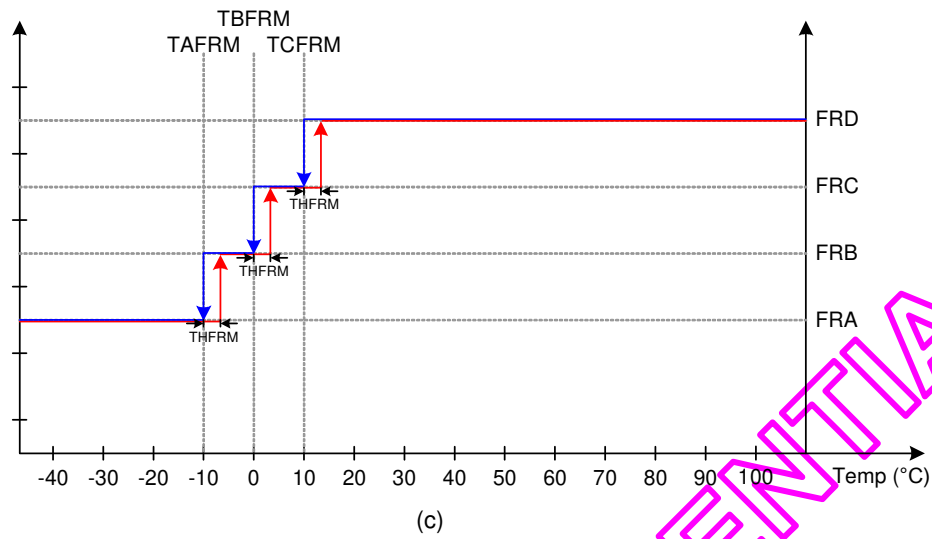


Fig. 10 Temperature Compensation of VCOM, VGH, and Frame Rate

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7. COMMAND

7.1 Command List

Instruction	ADD (HEX)	A0	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	Default (HEX)	Function		
DISOFF	11	0	1	↑	0	0	0	1	0	0	0	1		Display Off		
		1	1	↑	1	0	1	0	0	1	0	1				
DISON	12	0	1	↑	0	0	0	1	0	0	1	0		Display On		
		1	1	↑	1	0	1	0	0	1	0	1				
SLPOUT	13	0	1	↑	0	0	0	1	0	0	1	1		Sleep Out		
		1	1	↑	1	0	1	0	0	1	0	1				
SLPIN	14	0	1	↑	0	0	0	1	0	1	0	0		Sleep In		
		1	1	↑	1	0	1	0	0	1	0	1				
DINVOUT	15	0	1	↑	0	0	0	1	0	1	0	1		Display Invert Out		
		1	1	↑	1	0	1	0	0	1	0	1				
DINVIN	16	0	1	↑	0	0	0	1	0	1	1	0		Display Invert In		
		1	1	↑	1	0	1	0	0	1	0	1				
PTLIN	19	0	1	↑	0	0	0	1	1	0	0	1		Partial In		
		1	1	↑	1	0	1	0	0	1	0	1				
PTLOUT	1A	0	1	↑	0	0	0	1	1	0	1	0		Partial Out		
		1	1	↑	1	0	1	0	0	1	0	1				
BLIN	1B	0	1	↑	0	0	0	1	1	0	1	1		Blinking In		
		1	1	↑	1	0	1	0	0	1	0	1				
BLOUT	1C	0	1	↑	0	0	0	1	1	1	0	0		Blinking Out		
		1	1	↑	1	0	1	0	0	1	0	1				
MADCTL	21	0	1	↑	0	0	1	0	0	0	0	1		Memory Address Control		
		1	1	↑	0	0	0	0	0	MV	MY	MX			00	
		1	1	↑	1	0	1	0	0	1	0	1				
		1	1	↑	1	0	1	0	0	1	0	1				
		1	1	↑	1	0	1	0	0	1	0	1				
PASET	22	0	1	↑	0	0	1	0	0	0	1	0		Page Address Set		
		1	1	↑	PSA[7:0]										00	
		1	1	↑	PEA[7:0]										9F	
		1	1	↑	0	0	0	0	0	0	0	FrmA[1:0]			00	
CASET	23	0	1	↑	0	0	1	0	0	0	1	1		Column Address Set		
		1	1	↑	0	0	0	0	0	0	0	0			00	
		1	1	↑	CSA[7:0]										00	
		1	1	↑	0	0	0	0	0	0	0	0			00	
		1	1	↑	CEA[7:0]										EF	
STFRAME	24	0	1	↑	0	0	1	0	0	1	0	0		Start Frame Address		
		1	1	↑	0	0	0	0	0	0	SFrmA[1:0]	00				
		1	1	↑	1	0	1	0	0	1	0	1				



		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
BPPSEL	25	0	1	↑	0	0	1	0	0	1	0	1		
		1	1	↑	0	0	0	0	0	0	BppSel[1:0]		02	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
MDCTL	26	0	1	↑	0	0	1	0	0	1	1	0		
		1	1	↑	0	0	0	0	0	0	Dmask[1:0]		00	
		1	1	↑	MDSPA[7:0]							00		
		1	1	↑	MDEPA[7:0]							00		
PTLSET1	29	1	1	↑	1	0	1	0	0	1	0	1		
		0	1	↑	0	0	1	0	1	0	0	1		
		1	1	↑	0	0	0	0	0	0	0	0	Part1SL8	00
		1	1	↑	Part1SL[7:0]							00		
		1	1	↑	0	0	0	0	0	0	0	0	Part1EL8	00
PTLSET2	2A	1	1	↑	Part1EL[7:0]							00		
		0	1	↑	0	0	1	0	1	0	1	0		
		1	1	↑	0	0	0	0	0	0	0	0	Part2SL8	00
		1	1	↑	Part2SL[7:0]							00		
		1	1	↑	0	0	0	0	0	0	0	0	Part2EL8	00
BLSET	2B	1	1	↑	Part2EL[7:0]							00		
		0	1	↑	0	0	1	0	1	0	1	1		
		1	1	↑	BlinkCyc[7:0]							1D		
		1	1	↑	0	0	0	0	0	0	1	0	1	
		1	1	↑	1	0	1	0	0	1	0	1		
BLKFIL	31	1	1	↑	1	0	1	0	0	1	0	1		
		0	1	↑	1	1	0	0	0	0	0	1		
		1	1	↑	0	0	0	0	BFData[3:0]			00		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
RDRAM	39	0	1	↑	0	0	1	1	1	0	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	X	X	X	X	X	X	X	X		
		1	↑	1	Data[7:0]									
WRRAM	3A	0	1	↑	0	0	1	1	1	0	1	0		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	Data[7:0]									
VCM DAT	49	0	1	↑	0	1	0	0	1	0	0	1		
		1	1	↑	0	0	0	0	VcomS[3:0]			0E		
		1	1	↑	VcomD1[7:0]							00		
		1	1	↑	VcomD2[7:0]							00		
		1	1	↑	1	0	1	0	0	1	0	1		



UIDSET	4A	0	1	↑	0	1	0	0	1	0	1	0		User ID	
		1	1	↑	UID11[7:0]								00		
		1	1	↑	UID12[7:0]								00		
		1	1	↑	1	0	1	0	0	1	0	1			
RDERR	51	0	1	↑	0	1	0	1	0	0	0	1		Read Error Status	
		1	1	↑	1	0	1	0	0	1	0	1			
		1	↑	1	0	0	0	0	R13	0	0	0			
		1	↑	1	0	0	0	0	0	0	0	0			
RDSTAT	52	0	1	↑	0	1	0	1	0	0	1	0		Read Status	
		1	1	↑	1	0	1	0	0	1	0	1			
		1	↑	1	R1[7:5]				0	R1[3:0]					
		1	↑	1	0	R2[6:0]									
		1	↑	1	R3[7:0]										
		1	↑	1	R4[7:0]										
		1	↑	1	0	0	0	0	0	0	0	0	0		
RDREV	53	0	1	↑	0	1	0	1	0	0	1	0		Read Revision	
		1	1	↑	1	0	1	0	0	1	0	1			
		1	↑	1	R1[7:0]										
		1	↑	1	0	0	0	0	0	0	0	0	0		
		1	↑	1	0	0	0	0	0	0	0	0	0		
RDCRC	54	0	1	↑	0	1	0	1	0	1	0	0		Read CRC	
		1	1	↑	1	0	1	0	0	1	0	1			
		1	↑	1	CRC[15:8]										
		1	↑	1	CRC[7:0]										
RDUID	55	0	1	↑	0	1	0	1	0	1	0	1		Read User ID	
		1	1	↑	1	0	1	0	0	1	0	1			
		1	↑	1	R1[7:0]										
		1	↑	1	R2[7:0]										
		1	↑	1	0	0	0	0	0	0	0	0	0		
		1	↑	1	0	0	0	0	0	0	0	0	0		
		1	↑	1	0	0	0	0	0	0	0	0	0		
		1	↑	1	0	0	0	0	0	0	0	0	0		
		1	↑	1	0	0	0	0	0	0	0	0	0		
		1	↑	1	R9[7:0]										
		1	↑	1	RA[7:0]										
		1	↑	1	0	0	0	0	0	0	0	0	0		
		1	↑	1	0	0	0	0	0	0	0	0	0		
RDVCM DAT	59	0	1	↑	0	1	0	1	1	0	0	1		Read VCOM Data	
		1	1	↑	1	0	1	0	0	1	0	1			
		1	↑	1	R1[7:0]										
		1	↑	1	R2[7:0]										



		1	↑	1	0	0	0	0	0	0	0	0			
		1	↑	1	0	0	0	0	0	0	0	0	0		
		1	↑	1	R5[7:0]										
		1	↑	1	R6[7:0]										
		1	↑	1	R7[7:0]										
		1	↑	1	0	0	0	0	R83	R82	R81	R80			
CPSET	5A	0	1	↑	0	1	0	1	1	0	1	0		Charge Pump Setting	
		1	1	↑	0	CP2[2:0]			0	CP1[2:0]			20		
		1	1	↑	0	CP4[2:0]			0	CP3[2:0]			31		
		1	1	↑	1	0	1	0	0	1	0	1			
		1	1	↑	1	0	1	0	0	1	0	1			
SPI3WRCNT	5C	0	1	↑	0	1	0	1	1	1	0	0		SPI3 Write Memory Byte Counter	
		1	1	↑	Si3Mw[15:8]										96
		1	1	↑	Si3Mw[7:0]										00
		1	1	↑	1	0	1	0	0	1	0	1			
		1	1	↑	1	0	1	0	0	1	0	1			
SWRESET	5E	0	1	↑	0	1	0	1	1	1	1	0		Command Software Reset	
		1	1	↑	1	0	1	0	0	1	0	1			
PWRCTL	61	0	1	↑	0	1	1	0	0	0	0	1		Power Control	
		1	1	↑	BST3SR[1:0]		PclkRate[1:0]		BST4ON	BST3ON	BST2ON	BST1ON	40		
		1	1	↑	FOFNo[3:0]			0	SAP[2:0]			04			
		1	1	↑	0	0	0	0	0	1	0	02			
		1	1	↑	1	0	1	0	0	1	0	1			
BCLKSET	64	0	1	↑	0	1	1	0	0	1	0	0		Booster Clock Setting	
		1	1	↑	0	AVclCk_nd[2:0]		0	AVdCk_nd[2:0]			44			
		1	1	↑	0	VgICk_nd[2:0]		0	Vghclk_nd[2:0]			44			
		1	1	↑	0	AVclCk[2:0]		0	AVdCk[2:0]			44			
		1	1	↑	0	VgICk[2:0]		0	Vghclk[2:0]			44			
ACSET	69	0	1	↑	0	1	1	0	1	0	0	1		NLine	
		1	1	↑	0	0	0	0	ACDrive[3:0]			00			
		1	1	↑	1	0	1	0	0	1	0	1			
		1	1	↑	1	0	1	0	0	1	0	1			
		1	1	↑	1	0	1	0	0	1	0	1			
PWMCTRL	6C	0	1	↑	0	1	1	0	1	1	0	0		PWM Control Setting	
		1	1	↑	0	0	0	0	0	LOnTyp	0	LEDMD	00		
		1	1	↑	SLEDOOn[7:0]										00
		1	1	↑	ASLEDOOn[7:0]										80
		1	1	↑	ASLEDOF[7:0]										80
EVSET1	71	0	1	↑	0	1	1	1	0	0	0	1		Electronic Volumn Set 1	
		1	1	↑	VCOM[7:0]										22
		1	1	↑	0	0	VGHREG[5:0]					06			
		1	1	↑	0	0	0	VGLREG[4:0]					0F		
		1	1	↑	1	0	1	0	0	1	0	1			
EVSET2	72	0	1	↑	0	1	1	1	0	0	1	0		Electronic	



		1	1	↑	0	0	0	GVDD[4:0]					13	Volumn Set 2
		1	1	↑	0	0	0	GVCL[4:0]					13	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
RDTC	76	0	1	↑	0	1	1	1	0	1	1	0	Read TC Data	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	↑	1	0	0	0	0	0	0	0	0		XDTA8
		1	↑	1	XDTA[7:0]									
GAMSET4P1	81	0	1	↑	1	0	0	0	0	0	0	1	Gamma Set 4bpp Positive 1	
		1	1	↑	0	0	G4BPV0[5:0]					00		
		1	1	↑	0	0	G4BPV1[5:0]					04		
		1	1	↑	0	0	G4BPV2[5:0]					08		
		1	1	↑	0	0	G4BPV3[5:0]					0C		
GAMSET4P2	82	0	1	↑	1	0	0	0	0	0	1	0	Gamma Set 4bpp Positive 2	
		1	1	↑	0	0	G4BPV4[5:0]					10		
		1	1	↑	0	0	G4BPV5[5:0]					14		
		1	1	↑	0	0	G4BPV6[5:0]					18		
		1	1	↑	0	0	G4BPV7[5:0]					1C		
GAMSET4P3	83	0	1	↑	1	0	0	0	0	0	1	1	Gamma Set 4bpp Positive 3	
		1	1	↑	0	0	G4BPV8[5:0]					23		
		1	1	↑	0	0	G4BPV9[5:0]					27		
		1	1	↑	0	0	G4BPVA[5:0]					2B		
		1	1	↑	0	0	G4BPVB[5:0]					2F		
GAMSET4P4	84	0	1	↑	1	0	0	0	0	1	0	0	Gamma Set 4bpp Positive 4	
		1	1	↑	0	0	G4BPVC[5:0]					33		
		1	1	↑	0	0	G4BPVD[5:0]					37		
		1	1	↑	0	0	G4BPVE[5:0]					3B		
		1	1	↑	0	0	G4BPVF[5:0]					3F		
GAMSET2P	85	0	1	↑	1	0	0	0	0	1	0	1	Gamma Set 2bpp Positive	
		1	1	↑	0	0	G2BPV0[5:0]					00		
		1	1	↑	0	0	G2BPV1[5:0]					15		
		1	1	↑	0	0	G2BPV2[5:0]					2A		
		1	1	↑	0	0	G2BPV3[5:0]					3F		
GAMSET1	86	0	1	↑	1	0	0	0	1	1	0	Gamma Set 1bpp		
		1	1	↑	0	0	G1BPV0[5:0]						00	
		1	1	↑	0	0	G1BPV1[5:0]						3F	
		1	1	↑	0	0	G1BNV0[5:0]						00	
		1	1	↑	0	0	G1BNV1[5:0]						3F	
GAMSET4N1	89	0	1	↑	1	0	0	1	0	0	1	Gamma Set 4bpp Negative 1		
		1	1	↑	0	0	G4BNV0[5:0]						00	
		1	1	↑	0	0	G4BNV1[5:0]						04	
		1	1	↑	0	0	G4BNV2[5:0]						08	
		1	1	↑	0	0	G4BNV3[5:0]						0C	
GAMSET4N2	8A	0	1	↑	1	0	0	1	0	1	0	Gamma Set		



		1	1	↑	0	0	G4BNV4[5:0]					10	4bpp Negative 2		
		1	1	↑	0	0	G4BNV5[5:0]					14			
		1	1	↑	0	0	G4BNV6[5:0]					18			
		1	1	↑	0	0	G4BNV7[5:0]					1C			
GAMSET4N3	8B	0	1	↑	1	0	0	0	1	0	1	1	Gamma Set 4bpp Negative 3		
		1	1	↑	0	0	G4BNV8[5:0]					23			
		1	1	↑	0	0	G4BNV9[5:0]					27			
		1	1	↑	0	0	G4BNVA[5:0]					2B			
		1	1	↑	0	0	G4BNVB[5:0]					2F			
GAMSET4N4	8C	0	1	↑	1	0	0	0	1	1	0	0	Gamma Set 4bpp Negative 4		
		1	1	↑	0	0	G4BNVC[5:0]					33			
		1	1	↑	0	0	G4BNVD[5:0]					37			
		1	1	↑	0	0	G4BNVE[5:0]					3B			
		1	1	↑	0	0	G4BNVF[5:0]					3F			
GAMSET2N	8D	0	1	↑	1	0	0	0	1	1	0	1	Gamma Set 2bpp Negative		
		1	1	↑	0	0	G2BNV0[5:0]					00			
		1	1	↑	0	0	G2BNV1[5:0]					15			
		1	1	↑	0	0	G2BNV2[5:0]					2A			
		1	1	↑	0	0	G2BNV3[5:0]					3F			
DISAR	91	0	1	↑	1	0	0	1	0	0	0	1	Display Area		
		1	1	↑	0	0	0	0	0	0	0	DisLin8		01	
		1	1	↑	DisLin[7:0]									3F	
		1	1	↑	0	0	0	0	0	0	0	0		00	
		1	1	↑	1	1	1	0	1	1	1	1		EF	
DISSET1	92	0	1	↑	1	0	0	1	0	0	1	0	Display Set1		
		1	1	↑	HCikNo[7:0]									32	
		1	1	↑	BPN0[7:0]									02	
		1	1	↑	No_Blk	OSCO	Vsync_Sel	0	FPNo[11:8]					00	
		1	1	↑	FPNo[7:0]									01	
DISSET2	93	0	1	↑	1	0	0	1	0	0	1	1	Display Set2		
		1	1	↑	SOnT[7:0]									0A	
		1	1	↑	SOffT[7:0]									28	
		1	1	↑	GOnT[7:0]									0C	
		1	1	↑	GOffT[7:0]									26	
MTPPRG	99	0	1	↑	1	0	0	1	1	0	0	1	Multi Time PROM Program		
		1	1	↑	MTP_Func[7:0]									00	
		1	1	↑	1	0	1	0	0	1	0	1			
		1	1	↑	1	0	1	0	0	1	0	1			
		1	1	↑	1	0	1	0	0	1	0	1			
MTPOP	9A	0	1	↑	1	0	0	1	1	0	1	0	Multi Time PROM Operation		
		1	1	↑	0	0	0	0	0	0	Mtpcmd_rst	Prog_Mod		00	
		1	1	↑	1	0	1	0	0	1	0	1			
		1	1	↑	1	0	1	0	0	1	0	1			
		1	1	↑	1	0	1	0	0	1	0	1			



MTPRDEN	9B	0	1	↑	1	0	0	1	1	0	1	1		MTP Read Enable
		1	1	↑	1	0	1	0	0	1	0	1		
MTPWREN	9C	0	1	↑	1	0	0	1	1	1	0	0		MTP Write Enable
		1	1	↑	1	0	1	0	0	1	0	1		
GATESET	A2	0	1	↑	1	0	1	0	0	0	1	0		Gate Set
		1	1	↑	VGPP	0	0	ScanDir	0	0	ScanMod[1:0]		00	
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
		1	1	↑	1	0	1	0	0	1	0	1		
PTLSET3	AB	0	1	↑	1	0	1	0	1	0	1	1		Partial Set 3
		1	1	↑	0	NDisRefR[6:0]							00	
		1	1	↑	0	0	0	0	0	RTBFreq[2:0]		00		
		1	1	↑	NDisVCOM[1:0]		NDisGM[1:0]		0	0	NDisDM[1:0]		A1	
		1	1	↑	1	0	1	0	0	1	0	1		
RMWOUT	AC	0	1	↑	1	0	1	0	1	1	0	0		Read Modify
		1	1	↑	1	0	1	0	0	1	0	1		Write Out
RMWIN	AD	0	1	↑	1	0	1	0	1	1	0	1		Read Modify
		1	1	↑	1	0	1	0	0	1	0	1		Write In
TCPWMSY	B2	0	1	↑	1	0	1	1	0	0	1	0		TC PWM Sync Offset Set
		1	1	↑	TCAPS[7:0]							00		
		1	1	↑	TCBPS[7:0]							00		
		1	1	↑	TCCPS[7:0]							00		
TCPWMASON	B3	0	1	↑	1	0	1	1	0	0	1	1		TC PWM Async On Offset Set
		1	1	↑	TCAPAsOn[7:0]							00		
		1	1	↑	TCBPAsOn[7:0]							00		
		1	1	↑	TCCPAsOn[7:0]							00		
		1	1	↑	TCDPAsOn[7:0]							00		
TCPWMASOF	B4	0	1	↑	1	0	1	1	0	1	0	0		TC PWM Async Off Offset Set
		1	1	↑	TCAPAsOf[7:0]							00		
		1	1	↑	TCBPAsOf[7:0]							00		
		1	1	↑	TCCPAsOf[7:0]							00		
		1	1	↑	TCDPAsOf[7:0]							00		
TCVGH1	B5	0	1	↑	1	0	1	1	0	1	0	1		TC VGH Offset Set
		1	1	↑	0	TCAVGH[6:0]							00	
		1	1	↑	0	TCBVGH[6:0]							00	
		1	1	↑	0	TCCVGH[6:0]							00	
		1	1	↑	0	TCDVGH[6:0]							00	
TCVGH2	B6	0	1	↑	1	0	1	1	0	1	1	0		VGL Offset Set for VGH TC
		1	1	↑	TCAGlx[1:0]	TCAVGL[5:0]							00	
		1	1	↑	TCBGlx[1:0]	TCBVGL[5:0]							00	
		1	1	↑	TCCGlx[1:0]	TCCVGL[5:0]							00	
		1	1	↑	TCDGlx[1:0]	TCDVGL[5:0]							00	
TCVCOM	B9	0	1	↑	1	0	1	1	1	0	0	1		TCVCOM



		1	1	↑	0	0	0	TCAVCM[4:0]				00	Offset Set	
		1	1	↑	0	0	0	TCBVCM[4:0]				00		
		1	1	↑	0	0	0	TCCVCM[4:0]				00		
		1	1	↑	0	0	0	TCDVCM[4:0]				00		
SETTCGVD1	C1	0	1	↑	1	1	0	0	0	0	0	1	Set GVDD	
		1	1	↑	MTGVD1[3:0]				MTGVD0[3:0]				00	Temperature
		1	1	↑	MTGVD3[3:0]				MTGVD2[3:0]				00	Compensation
		1	1	↑	MTGVD5[3:0]				MTGVD4[3:0]				00	Gradient
		1	1	↑	MTGVD7[3:0]				MTGVD6[3:0]				00	Curves1
SETTCGVD2	C2	0	1	↑	1	1	0	0	0	0	1	0	Set GVDD	
		1	1	↑	MTGVD9[3:0]				MTGVD8[3:0]				00	Temperature
		1	1	↑	MTGVDB[3:0]				MTGVDA[3:0]				00	Compensation
		1	1	↑	MTGVDD[3:0]				MTGVDC[3:0]				00	Gradient
		1	1	↑	MTGVDF[3:0]				MTGVDE[3:0]				00	Curves2
SETTCGVD3	C3	0	1	↑	1	1	0	0	0	0	1	1	Set GVDD	
		1	1	↑	MTGVD11[3:0]				MTGVD10[3:0]				00	Temperature
		1	1	↑	0	0	0	0	THGVD[3:0]				04	Compensation
		1	1	↑	1	0	1	0	0	1	0	1	Gradient	
		1	1	↑	1	0	1	0	0	1	0	1	Curves3	
SETTCGVC1	C4	0	1	↑	1	1	0	0	0	1	0	0	Set GVCL	
		1	1	↑	MTGVC1[3:0]				MTGVC0[3:0]				00	Temperature
		1	1	↑	MTGVC3[3:0]				MTGVC2[3:0]				00	Compensation
		1	1	↑	MTGVC5[3:0]				MTGVC4[3:0]				00	Gradient
		1	1	↑	MTGVC7[3:0]				MTGVC6[3:0]				00	Curves1
SETTCGVC2	C5	0	1	↑	1	1	0	0	0	1	0	1	Set GVCL	
		1	1	↑	MTGVC9[3:0]				MTGVC8[3:0]				00	Temperature
		1	1	↑	MTGVCB[3:0]				MTGVCA[3:0]				00	Compensation
		1	1	↑	MTGVCD[3:0]				MTGVCC[3:0]				00	Gradient
		1	1	↑	MTGVCF[3:0]				MTGVCE[3:0]				00	Curves2
SETTCGVC3	C6	0	1	↑	1	1	0	0	0	1	1	0	Set GVCL	
		1	1	↑	MTGVC11[3:0]				MTGVC10[3:0]				00	Temperature
		1	1	↑	1	0	1	0	0	1	0	1	Compensation	
		1	1	↑	1	0	1	0	0	1	0	1	Gradient	
		1	1	↑	1	0	1	0	0	1	0	1	Curves3	
SETTCVGH	C7	0	1	↑	1	1	0	0	0	1	1	1	Set VGH Flag	
		1	1	↑	TAVGH[7:0]							00		
		1	1	↑	TBVGH[7:0]							00		
		1	1	↑	TCVGH[7:0]							00		
		1	1	↑	0	0	0	0	THVGH[3:0]					02
SETTCVCOM	C8	0	1	↑	1	1	0	0	1	0	0	0	Set TC VCOM Flag	
		1	1	↑	TAVCOM[7:0]							00		
		1	1	↑	TBVCOM[7:0]							00		
		1	1	↑	TCVCOM[7:0]							00		
		1	1	↑	0	0	0	0	THVCOM3					02



SETTCFRM	C9	0	1	↑	1	1	0	0	1	0	0	1		Set TC FRC Flag
		1	1	↑	TAFRM[7:0]							00		
		1	1	↑	TBFrm[7:0]							00		
		1	1	↑	TCFRM[7:0]							00		
		1	1	↑	0	0	0	0	THFRM[3:0]			02		
SETTCPWM	CB	0	1	↑	1	1	0	0	1	0	1	1		Set TC PWM Flag
		1	1	↑	TAPWM[7:0]							00		
		1	1	↑	TBPWM[7:0]							00		
		1	1	↑	TCPWM[7:0]							00		
		1	1	↑	0	0	0	0	THPWM[3:0]			02		
TCFP	CC	0	1	↑	1	1	0	0	1	1	0	0		Front Porch of Frame Rate TC Range Setting
		1	1	↑	TCAFP[7:0]							00		
		1	1	↑	TCBFP[7:0]							00		
		1	1	↑	TCCFP[7:0]							00		
		1	1	↑	TCDFP[7:0]							00		
TC1H	CD	0	1	↑	1	1	0	0	1	1	0	1		1H of Frame Rate TC Range Setting
		1	1	↑	TCAGLW[7:0]							00		
		1	1	↑	TCBGLW[7:0]							00		
		1	1	↑	TCCGLW[7:0]							00		
		1	1	↑	TCDGLW[7:0]							00		
TCBP	CE	0	1	↑	1	1	0	0	1	1	1	0		Back Porch of Frame Rate TC Range Setting
		1	1	↑	TCABP[7:0]							00		
		1	1	↑	TCBBP[7:0]							00		
		1	1	↑	TCCBP[7:0]							00		
		1	1	↑	TCDBP[7:0]							00		
TOSC	F4	0	1	↑	1	1	1	1	0	1	0	0		Command for MTP Control
		1	1	↑	0	0	0	0	0	0	0	0	00	
		1	1	↑	0	1	1	0	0	1	1	1	64	
		1	1	↑	1	1	1	MTPAuto	1	1	1	0	FC	
		1	1	↑	1	1	1	0	1	0	1	0	EA	



7.2 Command Description

7.2.1 Non-Operation

00H		Non-Operation										
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
NOP	0	1	↑	0	0	0	0	0	0	0	0	00
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> Non-operation. This command does not affect any operation. 											

7.2.2 Sleep Out

13H		Sleep out										
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPOUT	0	1	↑	0	0	0	1	0	0	1	1	13
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> It is required hardware reset at power-on. It is always required to input this command after hardware reset. 											

7.2.3 Sleep In

14H		Sleep in										
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SLPIN	0	1	↑	0	0	0	1	0	1	0	0	14
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> It is required hardware reset at power-on reset. It is always required to input this command after hardware reset. 											

7.2.4 Display Off

11H		Display off										
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISOFF	0	1	↑	0	0	0	1	0	0	0	1	11
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> Display off. 											

7.2.5 Display On

12H	Display on											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISON	0	1	↑	0	0	0	1	0	0	1	0	12
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> Start to display. SLPOUT command must be input before this command. After SLPOUT command, DISON command is waited until "display possible state" and this command is executed after wait time set by PWRCTL command. 											

7.2.6 Display Invert Out

15H	Display Invert out											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DINVIN	0	1	↑	0	0	0	1	0	1	0	1	15
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> Quit from display inverting state. It is enabled next frame after receiving the command. 											

7.2.7 Display Invert In

16H	Display Invert in											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DINVIN	0	1	↑	0	0	0	1	0	1	1	0	16
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> Inverts Display without re-writing display RAM. It is enabled next frame after receiving the command. 											

7.2.8 Blinking Out

1CH	Blinking out											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
BLOUT	0	1	↑	0	0	0	1	1	1	0	0	1C
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> Exit blinking display state. Frame address after exit is address set by STFRAME command. It is enable at frame changing of blinking cycle after the command. When WRRAM command is input after BLOUT, 2 NOP commands must be required before WRRAM. 											



7.2.9 Blinking In

1BH	Blinking in											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
BLIN	0	1	↑	0	0	0	1	1	0	1	1	1B
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> This command is used for blinking display by changing frame address. The blinking state is set by BLSET command. It is enable in next frame of the command input. During executing this command, RAM writing is invalid. In 1bpp mode with 4frames, other frames that is used by this command are valid to write RAM. 											

7.2.10 Start Frame Address

24H	Start Frame Address											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
STFRAME	0	1	↑	0	0	1	0	0	1	0	0	24
1st parameter	1	1	↑	0	0	0	0	0	0	SFrmA[1:0]		00
2nd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> Set frame address. SFrmA: Set start frame address 											

7.2.11 BPP Select

25H	BPP Selection											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
BPPSEL	0	1	↑	0	0	1	0	0	1	0	1	25
1st parameter	1	1	↑	0	0	0	0	0	0	BppSel[1:0]		02
2nd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> Set data format (bit per pixel) It is enabled next frame after receiving the command. It is possible to change 4bpp / 2bpp / 1bpp. It must be input during display off state, and display data must be written after changing BppSel[1:0] : Set data format (bit per pixel) <ul style="list-style-type: none"> 00: 1bpp (2 gray scale) 01: 2bpp (4 gray scale) 10: 4bpp (16 gray scale) 											



7.2.12 Memory Address Control

21H		Memory Address Control										
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MADCTL	0	1	↑	0	0	1	0	0	0	0	1	21
1st parameter	1	1	↑	0	0	0	0	0	MV	MY	MX	00
2nd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> Set about display data RAM. To access display RAM, it is required 1ms or more wait after input this command. MV: Select address incremental direction.(refer to 6.2.3) <ul style="list-style-type: none"> 0: Incremental column addr. 1: Incremental page addr. MY: Display data RAM page address (refer to 6.2.3) <ul style="list-style-type: none"> 0: Normal 1: Reverse MX: Display data RAM column address (refer to 6.2.3) <ul style="list-style-type: none"> 0: Normal 1: Reverse 											

7.2.13 Page Address Set

22H		Page Address Set										
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PASET	0	1	↑	0	0	1	0	0	0	1	0	22
1st parameter	1	1	↑	PSA[7:0]								00
2nd parameter	1	1	↑	PEA[7:0]								9F
3rd parameter	1	1	↑	0	0	0	0	0	0	FrmA[1:0]		00
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> Set page start address and page end address of display data RAM. PSA: Set page START address PEA: Set page END address FrmA: Set frame address Frame address range set by PASET command is depend on setting of BPPSEL command PSA < PEA 											



7.2.14 Column Address Set

23H	Column Address Set											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CASET	0	1	↑	0	0	1	0	0	0	1	1	23
1st parameter	1	1	↑	0	0	0	0	0	0	0	CSA8	00
2nd parameter	1	1	↑	CSA[7:0]								00
3rd parameter	1	1	↑	0	0	0	0	0	0	0	CEA8	00
4th parameter	1	1	↑	CEA[7:0]								EF
Description	<ul style="list-style-type: none"> ▪ Set column start address and column end address of display data RAM. ▪ CSA: Set column START address ▪ CEA: Set column END address ▪ CSA < CEA 											

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7.2.15 Block Fill

31H	Block Fill																																																																															
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																				
BLKFIL	0	1	↑	0	0	1	1	0	0	0	1	31																																																																				
1st parameter	1	1	↑	0	0	0	0	BFDData[3:0]				00																																																																				
2nd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5																																																																				
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5																																																																				
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5																																																																				
Description	<ul style="list-style-type: none"> Write set data to display data RAM area which set by CASET and PASET command. 60ms waiting time is required after BLKFIL command input. R23 of RDSTAT command is available to confirm display data RAM writing by BLKFIL command or not. During this term, prohibit DISAR, CASET, PASET, BPPSEL, WRRAM and RDRAM commands. When WRRAM or RDRAM command is input after BLKFIL, two NOP commands are required before WRRAM, RDRAM. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>BFDData[3:0]</th> <th>4bit data</th> <th>2bit data</th> <th>1bit data</th> </tr> </thead> <tbody> <tr><td>0h</td><td>0h</td><td>0h</td><td>0h</td></tr> <tr><td>1h</td><td>1h</td><td>1h</td><td>1h</td></tr> <tr><td>2h</td><td>2h</td><td>2h</td><td>0h</td></tr> <tr><td>3h</td><td>3h</td><td>3h</td><td>1h</td></tr> <tr><td>4h</td><td>4h</td><td>0h</td><td>0h</td></tr> <tr><td>5h</td><td>5h</td><td>1h</td><td>1h</td></tr> <tr><td>6h</td><td>6h</td><td>2h</td><td>0h</td></tr> <tr><td>7h</td><td>7h</td><td>3h</td><td>1h</td></tr> <tr><td>8h</td><td>8h</td><td>0h</td><td>0h</td></tr> <tr><td>9h</td><td>9h</td><td>1h</td><td>1h</td></tr> <tr><td>Ah</td><td>Ah</td><td>2h</td><td>0h</td></tr> <tr><td>Bh</td><td>Bh</td><td>3h</td><td>1h</td></tr> <tr><td>Ch</td><td>Ch</td><td>0h</td><td>0h</td></tr> <tr><td>Dh</td><td>Dh</td><td>1h</td><td>1h</td></tr> <tr><td>Eh</td><td>Eh</td><td>2h</td><td>0h</td></tr> <tr><td>Fh</td><td>Fh</td><td>3h</td><td>1h</td></tr> </tbody> </table>												BFDData[3:0]	4bit data	2bit data	1bit data	0h	0h	0h	0h	1h	1h	1h	1h	2h	2h	2h	0h	3h	3h	3h	1h	4h	4h	0h	0h	5h	5h	1h	1h	6h	6h	2h	0h	7h	7h	3h	1h	8h	8h	0h	0h	9h	9h	1h	1h	Ah	Ah	2h	0h	Bh	Bh	3h	1h	Ch	Ch	0h	0h	Dh	Dh	1h	1h	Eh	Eh	2h	0h	Fh	Fh	3h	1h
BFDData[3:0]	4bit data	2bit data	1bit data																																																																													
0h	0h	0h	0h																																																																													
1h	1h	1h	1h																																																																													
2h	2h	2h	0h																																																																													
3h	3h	3h	1h																																																																													
4h	4h	0h	0h																																																																													
5h	5h	1h	1h																																																																													
6h	6h	2h	0h																																																																													
7h	7h	3h	1h																																																																													
8h	8h	0h	0h																																																																													
9h	9h	1h	1h																																																																													
Ah	Ah	2h	0h																																																																													
Bh	Bh	3h	1h																																																																													
Ch	Ch	0h	0h																																																																													
Dh	Dh	1h	1h																																																																													
Eh	Eh	2h	0h																																																																													
Fh	Fh	3h	1h																																																																													



7.2.16 Blinking Set

2BH	Blinking Set																																																	
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																						
BLSET	0	1	↑	0	0	1	0	1	0	1	1	2B																																						
1st parameter	1	1	↑	BlinkCyc[7:0]								1D																																						
2nd parameter	1	1	↑	0	0	0	0	B1stF[1:0]		B2ndF[1:0]		01																																						
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5																																						
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5																																						
Description	<ul style="list-style-type: none"> This command is used to blink display to exchange frame RAMs. The blinking is fixed between 1st and 2nd frame addresses in 4bpp mode (120 lines or less are used) or 2bpp mode, and blinking is set by parameter 2 in 1bpp mode. It is enable in next frame of the command input. B1stF[1:0] and B2ndF[1:0]: Select blinking frame addresses. If invalid frame address is selected, it is return to initial value in 4bpp and 2bpp mode. <table border="1" style="margin-left: 40px;"> <thead> <tr> <th>BlinkCyc[7:0]</th> <th>Blinking Period</th> </tr> </thead> <tbody> <tr><td>00h</td><td>2 frame</td></tr> <tr><td>01h</td><td>2 frame</td></tr> <tr><td>02h</td><td>4 frame</td></tr> <tr><td>03h</td><td>4 frame</td></tr> <tr><td>...</td><td>...</td></tr> <tr><td>FDh</td><td>254 frame</td></tr> <tr><td>FEh</td><td>256 frame</td></tr> <tr><td>FFh</td><td>256 frame</td></tr> </tbody> </table> <table border="1" style="margin-left: 40px;"> <thead> <tr> <th>B1stF[1:0]</th> <th>1st frame addr.</th> </tr> </thead> <tbody> <tr><td>0h</td><td>0</td></tr> <tr><td>1h</td><td>1</td></tr> <tr><td>2h</td><td>2</td></tr> <tr><td>3h</td><td>3</td></tr> </tbody> </table> <table border="1" style="margin-left: 40px;"> <thead> <tr> <th>B2ndF[1:0]</th> <th>2nd frame addr.</th> </tr> </thead> <tbody> <tr><td>0h</td><td>0</td></tr> <tr><td>1h</td><td>1</td></tr> <tr><td>2h</td><td>2</td></tr> <tr><td>3h</td><td>3</td></tr> </tbody> </table>												BlinkCyc[7:0]	Blinking Period	00h	2 frame	01h	2 frame	02h	4 frame	03h	4 frame	FDh	254 frame	FEh	256 frame	FFh	256 frame	B1stF[1:0]	1st frame addr.	0h	0	1h	1	2h	2	3h	3	B2ndF[1:0]	2nd frame addr.	0h	0	1h	1	2h	2	3h	3
BlinkCyc[7:0]	Blinking Period																																																	
00h	2 frame																																																	
01h	2 frame																																																	
02h	4 frame																																																	
03h	4 frame																																																	
...	...																																																	
FDh	254 frame																																																	
FEh	256 frame																																																	
FFh	256 frame																																																	
B1stF[1:0]	1st frame addr.																																																	
0h	0																																																	
1h	1																																																	
2h	2																																																	
3h	3																																																	
B2ndF[1:0]	2nd frame addr.																																																	
0h	0																																																	
1h	1																																																	
2h	2																																																	
3h	3																																																	

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7.2.17 Write RAM

3AH		Write RAM										
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
WRRAM	0	1	↑	0	0	1	1	1	0	1	0	3A
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Write data	1	1	↑	Data[7:0]								
Description	<ul style="list-style-type: none"> After this WRRAM command, data is input at display area which is set by CASET and PASET command. RAM address is incremented automatically by WR signal. Column address, page address and frame address are set to start addresses by WRRAM command input. There is no limit to input data, and it is continued to be written until next command input. When the address arrives to end address, it is return to start address. 											

7.2.18 Read RAM

39H		Read RAM										
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDRAM	0	1	↑	0	0	1	1	1	0	0	1	39
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Dummy	1	↑	1	x	x	x	x	x	x	x	x	xx
Read data	1	↑	1	Data[7:0]								
Description	<ul style="list-style-type: none"> After this RDRAM command, data is read at display area which is set by CASET and PASET command. RAM address is incremented automatically by RD signal. Column address, page address and frame address are set to start addresses by RDRAM command input. There is no limit to read data, and it is continued to be read until next command input. When the address arrives to end address, it is return to start address. During BLKFIL command, data reading by RDRAM command is cancelled. 											

7.2.19 Display Area

91H		Display Area										
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISAR	0	1	↑	1	0	0	1	0	0	0	1	91
1st parameter	1	1	↑	0	0	0	0	0	0	0	DisLin[8]	01
2nd parameter	1	1	↑	DisLin[7:0]								3F
3rd parameter	1	1	↑	0	0	0	0	0	0	0	0	00
4th parameter	1	1	↑	1	1	1	0	1	1	1	1	EF
Description	<ul style="list-style-type: none"> Set display area lines. DisLin = number of display lines – 1 When number of display lines is decreased, porch term should be adjusted by DISET1 command to satisfy "1H =< 150us. 10 < DisLin < 320 											



7.2.20 Display Set1

92H	Display Set 1											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISSET1	0	1	↑	1	0	0	1	0	0	1	0	92
1st parameter	1	1	↑	HClkNo[7:0]								32
2nd parameter	1	1	↑	BPNo[7:0]								02
3rd parameter	1	1	↑	NorBlk	OSCO	0	0	FPNo[11:8]				00
4th parameter	1	1	↑	FPNo[7:0]								01

Description

- Set display conditions
- HClkNo = number of clocks in 1H – 1
- BPNo = number of back porch – 1
- FPNo = number of front porch – 1
- NorBlk: Select LCD type
 - 0: Normally black
 - 1: Normally white
- OSCO: OSCO pin function
 - 0: VSS output
 - 1: Clock output
- Frame rate = $\frac{10^6}{(BPNo + DisLin + FPNo + 3) \cdot (HClkNo + 1)}$ (Hz)

The diagram illustrates the timing of the display signals. The VSYNC signal is a single pulse with a duration of 1/FR. The HSYNC signal is a series of pulses, divided into three regions: Back Porch (BPNo+1), Display Lines (DisLin+1), and Front Porch (FPNo+1). The CL signal is a series of clock pulses with a duration of HClkNo+1. The diagram also shows a large 'CONFIDENTIAL' watermark and a 'COPY' watermark.



7.2.21 Display Set2

93H	Display Set 2											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
DISSET2	0	1	↑	1	0	0	1	0	0	1	1	93
1st parameter	1	1	↑	SOnT[7:0]								0A
2nd parameter	1	1	↑	SOffT[7:0]								28
3rd parameter	1	1	↑	GOnT[7:0]								0C
4th parameter	1	1	↑	GOffT[7:0]								26
Description	<ul style="list-style-type: none"> Set source and gate ON/OFF timing SOnT: Set source on timing by "number of clock from start – 1" SOffT: Set source off timing by "number of clock from start – 1" GOnT: Set gate on timing by "number of clock from start – 1" GOffT: Set gate off timing by "number of clock from start – 1" HClkNo > SOffT > GOffT 											

7.2.22 Partial Set 1

29H	Partial Set 1											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PTLSET1	0	1	↑	0	0	1	0	1	0	0	1	29
1st parameter	1	1	↑	Part1SL[8]								00
2nd parameter	1	1	↑	Part1SL[7:0]								00
3rd parameter	1	1	↑	1	0	1	0	0	1	0	Part1EL[8]	00
4th parameter	1	1	↑	Part1EL[7:0]								00
Description	<ul style="list-style-type: none"> It is used to display partially (line divided) in order to reduce power consumption. 2 display areas are settable. It is used with PTLSET2 and PTLSET3 command. 2 partial display areas are set within display lines set P1 and P2 of DISAR command. When 2nd area is not used, the start line and end line of the 2nd area must be set 511. Part1SL[8:0]: 1st partial display START line Part1EL[8:0]: 1st partial display END line When interlace is set, 1st partial display end line and 2nd partial display end line must not be set to 0, 1 and 2. 											



7.2.23 Partial Set 2

2AH	Partial Set 2											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PTLSET2	0	1	↑	0	0	1	0	1	0	1	0	2A
1st parameter	1	1	↑								Part2SL[8]	00
2nd parameter	1	1	↑	Part2SL[7:0]								00
3rd parameter	1	1	↑	1	0	1	0	0	1	0	Part2EL[8]	00
4th parameter	1	1	↑	Part2EL[7:0]								00
Description	<ul style="list-style-type: none"> It is used to display partially (line divided) in order to reduce power consumption. 2 display areas are settable. It is used with PTLSET1 and PTLSET3 command. 2 partial display areas are set within display lines set P1 and P2 of DISAR command. When 1st area is not used, the start line and end line of the 1st area must be set 511. Part2SL[8:0]: 1st partial display START line Part2EL[8:0]: 1st partial display END line When interlace is set, 1st partial display end line and 2nd partial display end line must not be set to 0, 1 and 2. 											

7.2.24 Partial Set 3

ABH	Partial Set 3												
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX	
PTLSET3	0	1	↑	1	0	1	0	1	0	1	1	AB	
1st parameter	1	1	↑	0	NDisRefR[6:0]								00
2nd parameter	1	1	↑	0	0	0	0	0	RTBFreq[2:0]			9F	
3rd parameter	1	1	↑	1	0	1	0	0	0	NDisDM[1:0]		A1	
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5	
Description	<p>It is used to display partially (line divided) in order to reduce power consumption. 2 display areas are settable. It is used with PTLSET1 and PTLSET2 command.</p>												



7.2.25 VCOM Offset Data

49H	VCOM Offset Data																																															
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																				
VCMDAT	0	1	↑	0	1	0	0	1	0	0	1	49																																				
1st parameter	1	1	↑	0	0	0	0	VcomS[3:0]				0E																																				
2nd parameter	1	1	↑	VcomD1[7:0]								00																																				
3rd parameter	1	1	↑	VcomD2[7:0]								00																																				
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5																																				
Description	<table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>VcomS[3:0]</th> <th>VCOM offset data select</th> </tr> </thead> <tbody> <tr> <td>0xxx</td> <td>No offset adjustment</td> </tr> <tr> <td>1x00</td> <td>Parameter 2 of this command (VCOM offset data1)</td> </tr> <tr> <td>1x01</td> <td>Parameter 3 of this command (VCOM offset data2)</td> </tr> <tr> <td>1110</td> <td>External MTP VCOM offset data1</td> </tr> <tr> <td>1111</td> <td>External MTP VCOM offset data2</td> </tr> <tr> <td>else</td> <td>TBD</td> </tr> </tbody> </table> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>VcomD1[7:0] and VcomD2[7:0]</th> <th>Offset</th> </tr> </thead> <tbody> <tr> <td>10000000</td> <td>-128</td> </tr> <tr> <td>10000001</td> <td>-127</td> </tr> <tr> <td>10000010</td> <td>-126</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>11111111</td> <td>-1</td> </tr> <tr> <td>00000000</td> <td>0</td> </tr> <tr> <td>00000001</td> <td>+1</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>01111110</td> <td>+126</td> </tr> <tr> <td>01111111</td> <td>+127</td> </tr> </tbody> </table>												VcomS[3:0]	VCOM offset data select	0xxx	No offset adjustment	1x00	Parameter 2 of this command (VCOM offset data1)	1x01	Parameter 3 of this command (VCOM offset data2)	1110	External MTP VCOM offset data1	1111	External MTP VCOM offset data2	else	TBD	VcomD1[7:0] and VcomD2[7:0]	Offset	10000000	-128	10000001	-127	10000010	-126	:	:	11111111	-1	00000000	0	00000001	+1	:	:	01111110	+126	01111111	+127
	VcomS[3:0]	VCOM offset data select																																														
	0xxx	No offset adjustment																																														
	1x00	Parameter 2 of this command (VCOM offset data1)																																														
	1x01	Parameter 3 of this command (VCOM offset data2)																																														
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	VcomD1[7:0] and VcomD2[7:0]	Offset																																														
	10000000	-128																																														
	10000001	-127																																														
	10000010	-126																																														
	:	:																																														
	11111111	-1																																														
00000000	0																																															
00000001	+1																																															
:	:																																															
01111110	+126																																															
01111111	+127																																															



7.2.26 User ID

4AH		User ID Set										
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
UIDSET	0	1	↑	0	1	0	0	1	0	1	0	4A
1st parameter	1	1	↑	UID11[7:0]								00
2nd parameter	1	1	↑	UID12[7:0]								00
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> Set user ID data to write Multi Time PROM UID11[7:0]: User ID1-1 data to write Multi Time PROM UID12[7:0]: User ID1-2 data to write Multi Time PROM 											

7.2.27 Multi Time PROM Mode

99H		Multi Time PROM Mode										
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MTPMOD	0	1	↑	1	0	0	1	1	0	0	1	99
1st parameter	1	1	↑	MTPMOD[7:0]								00
2nd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> MTPMOD[7:0]: Mode select <p>Read mode: BRM: F5h CAM: CFh FAM: 3Fh</p> <p>Program mode: 3Ah Erase mode: C5h</p>											



7.2.28 Multi Time PROM Operation

9AH		Multi Time PROM Operation										
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MTPOP	0	1	↑	1	0	0	1	1	0	1	0	9A
1st parameter	1	1	↑	0	0	0	0	0	0	0	Prog_Mod	00
2nd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> Prog_Mod: Program Mode <ul style="list-style-type: none"> 1: Enable 0: Disable 											

7.2.29 SPI3 Write Memory Byte Counter

5CH		SPI3 Write Memory Byte Counter										
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SPI3WRCNT	0	1	↑	0	1	0	1	1	1	0	0	5C
1st parameter	1	1	↑	Si3Mw[15:8]								01
2nd parameter	1	1	↑	Si3Mw[7:0]								8F
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> This command defines the numbers of data bytes written to DDRAM with 3-line SPI. Length of data byte = Si3Mw[15:0]+1 											

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7.2.30 Power Control

61H	Power Control											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PWRCTL	0	1	↑	0	1	1	0	0	0	0	1	61
1st parameter	1	1	↑	BST3SR[1:0]		PclkRate[1:0]		BST4ON	BST3ON	BST2ON	BST1ON	40
2nd parameter	1	1	↑	FOFNo[3:0]				0	SAMPSet[2:0]			04
3rd parameter	1	1	↑	0	0	0	0	0	0	1	0	02
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> Booster circuit control, source amp setting and booster clock frequency settings. This command must be input before SLPOUT command. BST3SR[1:0]: Step-up Rate of the 3rd booster setting 00, 01: "-1" 10: "-2" 11: "-3" PclkRate[1:0]: Pump clock rate. 2'b00: x1, 2'b01: x2, 2'b1x: x4 BST4ON ~ BST1ON: 4th ~ 1st booster On/Off setting 0: Booster off 1: Booster on FOFNo[3:0]: Force off frame, set waiting time by number of frames from sleep out to display on. SAMPSet[2:0]: Source Amplifier Setting 											

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7.2.31 Electronic Volume Set 1

71H	Electronic Volume Set 1											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
EVSET1	0	1	↑	0	1	1	1	0	0	0	1	71
1st parameter	1	1	↑	VCOM[7:0]								22
2nd parameter	1	1	↑	0	0	VGHREG[5:0]						06
3rd parameter	1	1	↑	0	0	0	VGLREG[4:0]					0F
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5

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Description

- Set each output voltages of built-in voltage regulators.
- $\begin{cases} VGL = BST3SR[1:0] \times VGLREG - 3V \\ VGH = 2 \times VGHREG - VGL \end{cases}$
- The voltage of VGL must be lower than AVCL.

VCOM[7:0]	VCOM (V)
00h	0
01h	-0.0125
02h	-0.0250
03h	-0.0375
:	:
9Eh	-1.9750
9Fh	-1.9875
A0h	-2.0000
:	:
FDh	-2.0000
FEh	-2.0000
FFh	-2.0000

VGHREG[5:0]	VGHREG (V)
00h	0
01h	1.5
02h	1.6
03h	1.7
:	:
27h	5.3
28h	5.4
29h	5.5
2Ah	5.5
:	:
3Eh	5.5
3Fh	5.5

VGLREG[4:0]	VGLREG (V)
00h	2.4
01h	2.5
02h	2.6
03h	2.7
:	:
1Dh	5.3
1Eh	5.4
1Fh	5.5

7.2.32 Electronic Volume Set 2



72H	Electronic Volume Set 1																																															
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																				
EVSET2	0	1	↑	0	1	1	1	0	0	1	0	72																																				
1st parameter	1	1	↑	0	0	0	GVDD[4:0]					13																																				
2nd parameter	1	1	↑	0	0	0	GVCL[4:0]					13																																				
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5																																				
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5																																				
Description	<ul style="list-style-type: none"> Set each output voltages of built-in voltage regulators. <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>GVDD[4:0]</th> <th>GVDD(V)</th> </tr> </thead> <tbody> <tr><td>00h</td><td>2.7</td></tr> <tr><td>01h</td><td>2.8</td></tr> <tr><td>02h</td><td>2.9</td></tr> <tr><td>03h</td><td>3.0</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>1Dh</td><td>5.6</td></tr> <tr><td>1Eh</td><td>5.7</td></tr> <tr><td>1Fh</td><td>5.8</td></tr> </tbody> </table> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>GVCL[4:0]</th> <th>GVCL(V)</th> </tr> </thead> <tbody> <tr><td>00h</td><td>-2.7</td></tr> <tr><td>01h</td><td>-2.8</td></tr> <tr><td>02h</td><td>-2.9</td></tr> <tr><td>03h</td><td>-3.0</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>1Dh</td><td>-5.6</td></tr> <tr><td>1Eh</td><td>-5.7</td></tr> <tr><td>1Fh</td><td>-5.8</td></tr> </tbody> </table>												GVDD[4:0]	GVDD(V)	00h	2.7	01h	2.8	02h	2.9	03h	3.0	:	:	1Dh	5.6	1Eh	5.7	1Fh	5.8	GVCL[4:0]	GVCL(V)	00h	-2.7	01h	-2.8	02h	-2.9	03h	-3.0	:	:	1Dh	-5.6	1Eh	-5.7	1Fh	-5.8
GVDD[4:0]	GVDD(V)																																															
00h	2.7																																															
01h	2.8																																															
02h	2.9																																															
03h	3.0																																															
:	:																																															
1Dh	5.6																																															
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GVCL[4:0]	GVCL(V)																																															
00h	-2.7																																															
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02h	-2.9																																															
03h	-3.0																																															
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1Eh	-5.7																																															
1Fh	-5.8																																															

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7.2.33 Booster Clock Setting

64H	Booster Clock Setting																													
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX																		
BCLKSET	0	1	↑	0	1	1	0	0	1	0	0	64																		
1st parameter	1	1	↑	0	AVclClk[2:0]			0	AVdClk[2:0]			44																		
2nd parameter	1	1	↑	0	VgIClk[2:0]			0	Vghclk[2:0]			44																		
3rd parameter	1	1	↑	0	AVclClk_nd[2:0]			0	AVdClk_nd[2:0]			44																		
4th parameter	1	1	↑	0	VgIClk_nd[2:0]			0	Vghclk_nd[2:0]			44																		
Description	AVclClk: AVCL normal display booster clock select AVdClk: AVDD normal display booster clock select VGHCK: VGH normal display booster clock select VGLCK: VGL normal display booster clock select AVclClk: AVCL partial non-display booster clock select AVdClk: AVDD partial non-display booster clock select VGHCK: VGH partial non-display booster clock select VGLCK: VGL partial non-display booster clock select																													
	<table border="1"> <thead> <tr> <th>HEX</th> <th>booster clock freq.</th> </tr> </thead> <tbody> <tr><td>0</td><td>4K</td></tr> <tr><td>1</td><td>7K</td></tr> <tr><td>2</td><td>10K</td></tr> <tr><td>3</td><td>15K</td></tr> <tr><td>4</td><td>20K</td></tr> <tr><td>5</td><td>31K</td></tr> <tr><td>6</td><td>40K</td></tr> <tr><td>7</td><td>62K</td></tr> </tbody> </table>												HEX	booster clock freq.	0	4K	1	7K	2	10K	3	15K	4	20K	5	31K	6	40K	7	62K
HEX	booster clock freq.																													
0	4K																													
1	7K																													
2	10K																													
3	15K																													
4	20K																													
5	31K																													
6	40K																													
7	62K																													

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7.2.34 Gate Set

A2H	Gate Set											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GATESET	0	1	↑	1	0	1	0	0	0	1	0	A2
1st parameter	1	1	↑	VGPP	0	0	ScanDir	0	0	ScanMod[1:0]		00
2nd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> ▪ Set line scan mode of gate driver. ▪ This command must be input before SLPOUT command. ▪ VGPP: Valid gate pin position <ul style="list-style-type: none"> 0: Inside 1: Outside ▪ ScanDir: Scan direction <ul style="list-style-type: none"> 0: Normal 1: Reverse ▪ ScanMode[1:0]: Scan mode (refer to 6.4) <ul style="list-style-type: none"> 00: scan mode 1 01: scan mode 2 10: scan mode 3 11: scan mode 4 											

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7.2.35 Read Status

52H	Read Status											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDSTAT	0	1	↑	0	1	0	1	0	0	1	0	52
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
1st read data	1	↑	1	R17	R16	R15	0	R13	R12	R11	R10	
2nd read data	1	↑	1	0	R26	R25	R24	R23	R22	R21	R20	
3rd read data	1	↑	1	R37	R36	R35	R34	R33	R32	R31	R30	
4th read data	1	↑	1	R47	R46	R45	R44	R43	R42	R41	R40	
Description	<ul style="list-style-type: none"> ▪ Display Status (1/0) <ul style="list-style-type: none"> R10: '0': DISOFF '1': DISON R11: '0': SLPIN '1': SLPOUT R12: '0': PTLOUT '1': PTLIN R13: '0': DINVOUT '1': DINVIN R[17, 16, 15] = [1bpp, 2bpp, 4bpp] ▪ RAM Status <ul style="list-style-type: none"> R20: Page address increment '0': Normal '1': Reverse R21: Column address increment '0': Normal '1': Reverse R22: Scan direction '0': Column '1': Page R23: BLKFIL '0': Command not executed '1': Command executed R24: '0': BLOUT '1': BLIN R26, R25: Bit operation of start and end page (01: AND, 10: OR) ▪ R3[7:0]: Mask data of writing start page ▪ R4[7:0]: Mask data of writing end page 											

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7.2.36 Read Revision

53H		Read Revision										
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDREV	0	1	↑	0	1	0	1	0	0	1	1	53
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
1st read data	1	↑	1	R17	R16	R15	R14	R13	R12	R11	R10	
Description	▪ R1[7:0]: Read IC Revision											

7.2.37 Read CRC

54H		Read CRC										
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDCRC	0	1	↑	0	1	0	1	0	1	0	0	54
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
1st read data	1	↑	1	CRC[15:8]								
2nd read data	1	↑	1	CRC[7:0]								
Description	<ul style="list-style-type: none"> ▪ It is possible to confirm the data by comparing the CRC calculation result from ST7512 with the expected value on MCU side. ▪ This command reads the CRC calculation result of all input data, including commands, parameters, NOP, even invalid codes. ▪ This command is input after transferring input data, then the CRC calculation result can be read. ▪ The CRC calculation result includes this command code and parameter. ▪ The CRC value is initialized by reset (hardware reset and software reset). ▪ The CRC value will be reinitialized after this command executed. The initial value is FFFFh. <p>CRC calculation Polynomial: $X^{16} + X^{12} + X^5 + 1$ Parity length: 16 bits</p>											

7.2.38 Read User ID

55H		Read User ID										
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDUID	0	1	↑	0	1	0	1	0	1	0	1	55
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
1st read data	1	↑	1	R17	R16	R15	R14	R13	R12	R11	R10	
2nd read data	1	↑	1	R27	R26	R25	R24	R23	R22	R21	R20	
:	:	:	:	:	:	:	:	:	:	:	:	
9th read data	1	↑	1	R97	R96	R95	R94	R93	R92	R91	R90	
10th read data	1	↑	1	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0	



Description	<ul style="list-style-type: none"> ▪ R1[7:0]: MTP UID1-1 ▪ R2[7:0]: MTP UID1-2 ▪ R9[7:0]: UIDSET Register UID1-1 ▪ RA[7:0]: UIDSET Register UID1-2
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7.2.39 Read VCOM Data

59H	Read VCOM Data											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDVCM DAT	0	1	↑	0	1	0	1	1	0	0	1	59
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
1st read data	1	↑	1	R17	R16	R15	R14	R13	R12	R11	R10	
2nd read data	1	↑	1	R27	R26	R25	R24	R23	R22	R21	R20	
:	:	:	:	:	:	:	:	:	:	:	:	
5th read data	1	↑	1	R57	R56	R55	R54	R53	R52	R51	R50	
6th read data	1	↑	1	R67	R66	R65	R64	R63	R62	R61	R60	
7th read data	1	↑	1	R77	R76	R75	R74	R73	R72	R71	R70	
8th read data	1	↑	1	x	x	x	x	R83	R82	R81	R80	
Description	<ul style="list-style-type: none"> ▪ R1[7:0]: MTP VCOM offset value1 ▪ R2[7:0]: MTP VCOM offset value2 ▪ R5[7:0]: VCMDAT register VCOM offset value1 ▪ R6[7:0]: VCMDAT register VCOM offset value2 ▪ R7[7:0]: VCOM electric volume (EVSET1 2nd parameter + VCMDAT) ▪ R8[3:0]: VCOM offset data reference point 											

7.2.40 Gamma Set 4bpp Positive 1

81H	Gamma Set 4bpp Positive 1											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET4P1	0	1	↑	1	0	0	0	0	0	0	1	81
1st parameter	1	1	↑	0	0	G4BPV0[5:0]					00	
2nd parameter	1	1	↑	0	0	G4BPV1[5:0]					04	
3rd parameter	1	1	↑	0	0	G4BPV2[5:0]					08	
4th parameter	1	1	↑	0	0	G4BPV3[5:0]					0C	
Description	<ul style="list-style-type: none"> ▪ Set LCD gamma voltage setting of positive polarity in 4bpp mode. ▪ This command must be input before SLPOUT. ▪ G4BPV0: V0 voltage setting (positive polarity) ▪ G4BPV1: V1 voltage setting (positive polarity) ▪ G4BPV2: V2 voltage setting (positive polarity) ▪ G4BPV3: V3 voltage setting (positive polarity) 											



7.2.41 Gamma Set 4bpp Positive 2

82H	Gamma Set 4bpp Positive 2											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET4P2	0	1	↑	1	0	0	0	0	0	1	0	82
1st parameter	1	1	↑	0	0	G4BPV4[5:0]						10
2nd parameter	1	1	↑	0	0	G4BPV5[5:0]						14
3rd parameter	1	1	↑	0	0	G4BPV6[5:0]						18
4th parameter	1	1	↑	0	0	G4BPV7[5:0]						1C
Description	<ul style="list-style-type: none"> Set LCD gamma voltage setting of positive polarity in 4bpp mode. This command must be input before SLPOUT. G4BPV4: V4 voltage setting (positive polarity) G4BPV5: V5 voltage setting (positive polarity) G4BPV6: V6 voltage setting (positive polarity) G4BPV7: V7 voltage setting (positive polarity) 											

7.2.42 Gamma Set 4bpp Positive 3

83H	Gamma Set 4bpp Positive 3											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET4P3	0	1	↑	1	0	0	0	0	0	1	1	83
1st parameter	1	1	↑	0	0	G4BPV8[5:0]						23
2nd parameter	1	1	↑	0	0	G4BPV9[5:0]						27
3rd parameter	1	1	↑	0	0	G4BPV10[5:0]						2B
4th parameter	1	1	↑	0	0	G4BPV11[5:0]						2F
Description	<ul style="list-style-type: none"> Set LCD gamma voltage setting of positive polarity in 4bpp mode. This command must be input before SLPOUT. G4BPV8: V8 voltage setting (positive polarity) G4BPV9: V9 voltage setting (positive polarity) G4BPV10: V10 voltage setting (positive polarity) G4BPV11: V11 voltage setting (positive polarity) 											



7.2.43 Gamma Set 4bpp Positive 4

84H	Gamma Set 4bpp Positive 4											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET4P4	0	1	↑	1	0	0	0	0	1	0	0	84
1st parameter	1	1	↑	0	0	G4BPVC[5:0]						33
2nd parameter	1	1	↑	0	0	G4BPVD[5:0]						37
3rd parameter	1	1	↑	0	0	G4BPVE[5:0]						3B
4th parameter	1	1	↑	0	0	G4BPVF[5:0]						3F
Description	<ul style="list-style-type: none"> Set LCD gamma voltage setting of positive polarity in 4bpp mode. This command must be input before SLPOUT. G4BPV12: V12 voltage setting (positive polarity) G4BPV13: V13 voltage setting (positive polarity) G4BPV14: V14 voltage setting (positive polarity) G4BPV15: V15 voltage setting (positive polarity) 											

7.2.44 Gamma Set 2bpp Positive

85H	Gamma Set 2bpp Positive											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET2P	0	1	↑	1	0	0	0	0	1	0	1	85
1st parameter	1	1	↑	0	0	G2BPV0[5:0]						00
2nd parameter	1	1	↑	0	0	G2BPV1[5:0]						15
3rd parameter	1	1	↑	0	0	G2BPV2[5:0]						2A
4th parameter	1	1	↑	0	0	G2BPV3[5:0]						3F
Description	<ul style="list-style-type: none"> Set LCD gamma voltage setting of positive polarity in 2bpp mode. This command must be input before SLPOUT. G2BPV0: V0 voltage setting (positive polarity) G2BPV1: V1 voltage setting (positive polarity) G2BPV2: V2 voltage setting (positive polarity) G2BPV3: V3 voltage setting (positive polarity) 											

7.2.45 Gamma Set 1bpp

86H	Gamma Set 1bpp											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET	0	1	↑	1	0	0	0	0	1	1	0	86
1st parameter	1	1	↑	0	0	G1BPV0[5:0]						00
2nd parameter	1	1	↑	0	0	G1BPV1[5:0]						3F
3rd parameter	1	1	↑	0	0	G1BNV0[5:0]						00
4th parameter	1	1	↑	0	0	G1BNV1[5:0]						3F
Description	<ul style="list-style-type: none"> Set LCD gamma voltage setting of positive and negative polarity in 1bpp mode. This command must be input before SLPOUT. G1BPV0: V0 voltage setting (positive polarity) G1BPV1: V1 voltage setting (positive polarity) G1BNV0: V0 voltage setting (negative polarity) G1BNV1: V1 voltage setting (negative polarity) 											

7.2.46 Gamma Set 4bpp Negative 1

89H	Gamma Set 4bpp Negative 1											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET4N1	0	1	↑	1	0	0	0	1	0	0	1	89
1st parameter	1	1	↑	0	0	G4BNV0[5:0]						00
2nd parameter	1	1	↑	0	0	G4BNV1[5:0]						04
3rd parameter	1	1	↑	0	0	G4BNV2[5:0]						08
4th parameter	1	1	↑	0	0	G4BNV3[5:0]						0C
Description	<ul style="list-style-type: none"> Set LCD gamma voltage setting of negative polarity in 4bpp mode. This command must be input before SLPOUT. G4BNV0: V0 voltage setting (negative polarity) G4BNV1: V1 voltage setting (negative polarity) G4BNV2: V2 voltage setting (negative polarity) G4BNV3: V3 voltage setting (negative polarity) 											



7.2.47 Gamma Set 4bpp Negative 2

8AH	Gamma Set 4bpp Negative 2											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET4N2	0	1	↑	1	0	0	0	1	0	1	0	8A
1st parameter	1	1	↑	0	0	G4BNV4[5:0]						10
2nd parameter	1	1	↑	0	0	G4BNV5[5:0]						14
3rd parameter	1	1	↑	0	0	G4BNV6[5:0]						18
4th parameter	1	1	↑	0	0	G4BNV7[5:0]						1C
Description	<ul style="list-style-type: none"> Set LCD gamma voltage setting of negative polarity in 4bpp mode. This command must be input before SLPOUT. G4BNV4: V4 voltage setting (negative polarity) G4BNV5: V5 voltage setting (negative polarity) G4BNV6: V6 voltage setting (negative polarity) G4BNV7: V7 voltage setting (negative polarity) 											

7.2.48 Gamma Set 4bpp Negative 3

8BH	Gamma Set 4bpp Negative 3											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET4N3	0	1	↑	1	0	0	0	1	0	1	1	8B
1st parameter	1	1	↑	0	0	G4BNV8[5:0]						23
2nd parameter	1	1	↑	0	0	G4BNV9[5:0]						27
3rd parameter	1	1	↑	0	0	G4BNVA[5:0]						2B
4th parameter	1	1	↑	0	0	G4BNVB[5:0]						2F
Description	<ul style="list-style-type: none"> Set LCD gamma voltage setting of negative polarity in 4bpp mode. This command must be input before SLPOUT. G4BNV8: V8 voltage setting (negative polarity) G4BNV9: V9 voltage setting (negative polarity) G4BNVA: V10 voltage setting (negative polarity) G4BNVB: V11 voltage setting (negative polarity) 											



7.2.49 Gamma Set 4bpp Negative 4

8CH	Gamma Set 4bpp Negative 4											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET4N4	0	1	↑	1	0	0	0	1	1	0	0	8C
1st parameter	1	1	↑	0	0	G4BNVC[5:0]						33
2nd parameter	1	1	↑	0	0	G4BNVD[5:0]						37
3rd parameter	1	1	↑	0	0	G4BNVE[5:0]						3B
4th parameter	1	1	↑	0	0	G4BNVF[5:0]						3F
Description	<ul style="list-style-type: none"> ▪ Set LCD gamma voltage setting of negative polarity in 4bpp mode. ▪ This command must be input before SLPOUT. ▪ G4BNVC: V12 voltage setting (negative polarity) ▪ G4BNVD: V13 voltage setting (negative polarity) ▪ G4BNVE: V14 voltage setting (negative polarity) ▪ G4BNVF: V15 voltage setting (negative polarity) 											

7.2.50 Gamma Set 2bpp Negative

8DH	Gamma Set 2bpp Negative											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
GAMSET2N	0	1	↑	1	0	0	0	1	1	0	1	8D
1st parameter	1	1	↑	0	0	G2BNV0[5:0]						00
2nd parameter	1	1	↑	0	0	G2BNV1[5:0]						15
3rd parameter	1	1	↑	0	0	G2BNV2[5:0]						2A
4th parameter	1	1	↑	0	0	G2BNV3[5:0]						3F
Description	<ul style="list-style-type: none"> ▪ Set LCD gamma voltage setting of negative polarity in 2bpp mode. ▪ This command must be input before SLPOUT. ▪ G2BNV0: V0 voltage setting (negative polarity) ▪ G2BNV1: V1 voltage setting (negative polarity) ▪ G2BNV2: V2 voltage setting (negative polarity) ▪ G2BNV3: V3 voltage setting (negative polarity) 											



7.2.51 Read Modify Write In

ADH	Read Modify Write in											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RMWIN	0	1	↑	1	0	1	0	1	1	0	1	AD
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> Read modify write mode in Only valid in 6800/8080 											

7.2.52 MTP Read Enable

9BH	MTP Read Enable											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MTPRDEN	0	1	↑	1	0	0	1	1	0	1	1	9B
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> MTP read enable 											

7.2.53 MTP Write Enable

9CH	MTP White Enable											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
MTPWREN	0	1	↑	1	0	0	1	1	1	0	0	9C
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ MTP write enable											

7.2.54 Partial Out

1AH	Partial out											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PTLOUT	0	1	↑	0	0	0	1	1	0	1	0	1A
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Escape from partial display mode.											

7.2.55 Partial In

19H	Partial in											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
PTLIN	0	1	↑	0	0	0	1	1	0	0	1	19
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Enter into partial display mode.											

7.2.56 Read Modify Write Out

ACH	Read Modify Write out											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RMWOUT	0	1	↑	1	0	1	0	1	1	0	0	AC
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ Read modify write mode out ▪ Only valid in 6800/8080											

7.2.57 Software Reset

5EH	Software Reset											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SWRESET	0	1	↑	0	1	0	1	1	1	1	0	5E
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	▪ This command make a reset as same as hardware reset. ▪ It is required Hardware reset at power-on reset. ▪ It is always required to input this command after hardware reset.											



7.2.58 Read TC Data

76H	Read TC Data											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
RDTC	0	1	↑	0	1	1	1	0	1	1	0	76
1st parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
1st read data	1	↑	1	0	0	0	0	0	0	0	XDTA[8]	
2nd read data	1	↑	1	XDTA[7:0]								
Description	<ul style="list-style-type: none"> Temperature = $-40 + 0.5 \times \text{XDTA}[8:0]$ ($\pm 4^*$) °C * The variation of temperature read from the internal sensor may be affected by the conditions of IC operation. 											

7.2.59 Command for MTP Autoload Control

F4H	Command for MTP Autoload Control											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
TCSET	0	1	↑	1	1	1	1	0	1	0	0	F4
1st parameter	1	↑	1	0	0	0	0	0	0	0	0	00
2nd parameter	1	↑	1	0	1	1	0	0	1	1	1	64
3rd parameter	1	↑	1	1	1	1	MTPAuto	1	1	1	0	FC
4th parameter	1	↑	1	1	1	1	0	1	0	1	0	EA
Description	<ul style="list-style-type: none"> MTPAuto: MTP autoload 0: off 1: on 											

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7.2.60 TCVCOM Offset Set

B9H	TCVCOM Offset Set																																																																													
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX																																																																		
TCSET	0	1	↑	1	0	1	1	1	0	0	1	B9																																																																		
1st parameter	1	1	↑	0	0	0	TCAVCM[4:0]					00																																																																		
2nd parameter	1	1	↑	0	0	0	TCBVCM[4:0]					00																																																																		
3rd parameter	1	1	↑	0	0	0	TCCVCM[4:0]					00																																																																		
4th parameter	1	1	↑	0	0	0	TCDVCM[4:0]					00																																																																		
Description	<ul style="list-style-type: none"> • TCAVCM[4:0]: TC offset for VCOM of temperature zone A • TCBVCM[4:0]: TC offset for VCOM of temperature zone B • TCCVCM[4:0]: TC offset for VCOM of temperature zone C • TCDVCM[4:0]: TC offset for VCOM of temperature zone D <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>TCxVCM[4:0] x=A, B, C, D</th> <th>Offset</th> </tr> </thead> <tbody> <tr><td>10000</td><td>-16</td></tr> <tr><td>10001</td><td>-15</td></tr> <tr><td>10010</td><td>-14</td></tr> <tr><td>10011</td><td>-13</td></tr> <tr><td>10100</td><td>-12</td></tr> <tr><td>10101</td><td>-11</td></tr> <tr><td>10110</td><td>-10</td></tr> <tr><td>10111</td><td>-9</td></tr> <tr><td>11000</td><td>-8</td></tr> <tr><td>11001</td><td>-7</td></tr> <tr><td>11010</td><td>-6</td></tr> <tr><td>11011</td><td>-5</td></tr> <tr><td>11100</td><td>-4</td></tr> <tr><td>11101</td><td>-3</td></tr> <tr><td>11110</td><td>-2</td></tr> <tr><td>11111</td><td>-1</td></tr> <tr><td>00000</td><td>0</td></tr> <tr><td>00001</td><td>+1</td></tr> <tr><td>00010</td><td>+2</td></tr> <tr><td>00011</td><td>+3</td></tr> <tr><td>00100</td><td>+4</td></tr> <tr><td>00101</td><td>+5</td></tr> <tr><td>00110</td><td>+6</td></tr> <tr><td>00111</td><td>+7</td></tr> <tr><td>01000</td><td>+8</td></tr> <tr><td>01001</td><td>+9</td></tr> <tr><td>01010</td><td>+10</td></tr> <tr><td>01011</td><td>+11</td></tr> <tr><td>01100</td><td>+12</td></tr> <tr><td>01101</td><td>+13</td></tr> <tr><td>01110</td><td>+14</td></tr> <tr><td>01111</td><td>+15</td></tr> </tbody> </table>												TCxVCM[4:0] x=A, B, C, D	Offset	10000	-16	10001	-15	10010	-14	10011	-13	10100	-12	10101	-11	10110	-10	10111	-9	11000	-8	11001	-7	11010	-6	11011	-5	11100	-4	11101	-3	11110	-2	11111	-1	00000	0	00001	+1	00010	+2	00011	+3	00100	+4	00101	+5	00110	+6	00111	+7	01000	+8	01001	+9	01010	+10	01011	+11	01100	+12	01101	+13	01110	+14	01111	+15
TCxVCM[4:0] x=A, B, C, D	Offset																																																																													
10000	-16																																																																													
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7.2.61 TC VGHREG Offset Set

B5H	TC VGHREG Offset Set																															
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX																				
TCVGH1	0	1	↑	1	0	1	1	0	1	0	1	B5																				
1st parameter	1	1	↑	0	TCAVGH[6:0]							00																				
2nd parameter	1	1	↑	0	TCBVGH[6:0]							00																				
3rd parameter	1	1	↑	0	TCCVGH[6:0]							00																				
4th parameter	1	1	↑	0	TCDVGH[6:0]							00																				
Description	<ul style="list-style-type: none"> • TCAVGH[6:0]: TC offset for VGHREG of temperature zone A • TCBVGH[6:0]: TC offset for VGHREG of temperature zone B • TCCVGH[6:0]: TC offset for VGHREG of temperature zone C • TCDVGH[6:0]: TC offset for VGHREG of temperature zone D <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>TCxVGH[6:0] x=A, B, C, D</th> <th>Offset</th> </tr> </thead> <tbody> <tr><td>1000000</td><td>-64</td></tr> <tr><td>1000001</td><td>-63</td></tr> <tr><td>1000010</td><td>-62</td></tr> <tr><td>1111111</td><td>-1</td></tr> <tr><td>0000000</td><td>0</td></tr> <tr><td>0000001</td><td>+1</td></tr> <tr><td>:</td><td>:</td></tr> <tr><td>0111110</td><td>+62</td></tr> <tr><td>0111111</td><td>+63</td></tr> </tbody> </table>												TCxVGH[6:0] x=A, B, C, D	Offset	1000000	-64	1000001	-63	1000010	-62	1111111	-1	0000000	0	0000001	+1	:	:	0111110	+62	0111111	+63
TCxVGH[6:0] x=A, B, C, D	Offset																															
1000000	-64																															
1000001	-63																															
1000010	-62																															
1111111	-1																															
0000000	0																															
0000001	+1																															
:	:																															
0111110	+62																															
0111111	+63																															

7.2.62 Set GVDD Temperature Compensation Gradient Curves1

C1H	Set GVDD Temperature Compensation Gradient Curves1											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SETTCGVD1	0	1	↑	1	1	0	0	0	0	0	1	C1
1st parameter	1	1	↑	MTGVD1[3:0]			MTGVD0[3:0]					00
2nd parameter	1	1	↑	MTGVD3[3:0]			MTGVD2[3:0]					00
3rd parameter	1	1	↑	MTGVD5[3:0]			MTGVD4[3:0]					00
4th parameter	1	1	↑	MTGVD7[3:0]			MTGVD6[3:0]					00
Description	<ul style="list-style-type: none"> • MTGVDx[3]: TCx(x=0~7) polarity 1: Positive, 0: Negative • MTGVD0[2:0]: Set GVDD Gradient of TC0 Curves -40~-32°C • MTGVD1[2:0]: Set GVDD Gradient of TC1 Curves -32~-24°C • MTGVD2[2:0]: Set GVDD Gradient of TC2 Curves -24~-16°C • MTGVD3[2:0]: Set GVDD Gradient of TC3 Curves -16~-8°C • MTGVD4[2:0]: Set GVDD Gradient of TC4 Curves -8~0°C • MTGVD5[2:0]: Set GVDD Gradient of TC5 Curves 0~8°C • MTGVD6[2:0]: Set GVDD Gradient of TC6 Curves 8~16°C • MTGVD7[2:0]: Set GVDD Gradient of TC7 Curves 16~24°C 											



7.2.63 Set GVDD Temperature Compensation Gradient Curves2

C2H	Set GVDD Temperature Compensation Gradient Curves2											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SETTCGVDD2	0	1	↑	1	1	0	0	0	0	1	0	C2
1st parameter	1	1	↑	MTGVD9[3:0]				MTGVD8[3:0]				00
2nd parameter	1	1	↑	MTGVDB[3:0]				MTGVDA[3:0]				00
3rd parameter	1	1	↑	MTGVDD[3:0]				MTGVDC[3:0]				00
4th parameter	1	1	↑	MTGVDF[3:0]				MTGVDE[3:0]				00
Description	<ul style="list-style-type: none"> • MTGVDx[3]: TCx(x=8~F) polarity 1: Positive, 0: Negative • MTGVD8[2:0]: Set GVDD Gradient of TC8 Curves 24~32°C • MTGVD9[2:0]: Set GVDD Gradient of TC9 Curves 32~40°C • MTGVDA[2:0]: Set GVDD Gradient of TCA Curves 40~48°C • MTGVDB[2:0]: Set GVDD Gradient of TCB Curves 48~56°C • MTGVDC[2:0]: Set GVDD Gradient of TCC Curves 56~64°C • MTGVDD[2:0]: Set GVDD Gradient of TCD Curves 64~72°C • MTGVDE[2:0]: Set GVDD Gradient of TCE Curves 72~80°C • MTGVDF[2:0]: Set GVDD Gradient of TCF Curves 80~88°C 											

7.2.64 Set GVDD Temperature Compensation Gradient Curves3

C3H	Set GVDD Temperature Compensation Gradient Curves3																									
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX														
SETTCGVDD3	0	1	↑	1	1	0	0	0	0	1	1	C3														
1st parameter	1	1	↑	MTGVD11[3:0]				MTGVD10[3:0]				00														
2nd parameter	1	1	↑	0	0	THGVD[5:0]					04															
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5														
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5														
Description	<ul style="list-style-type: none"> • MTGVDx[3]: TCx(x=10~11) polarity 1: Positive, 0: Negative • MTGVD10[2:0]: Set GVDD Gradient of TC10 Curves 88~96°C • MTGVD11[2:0]: Set GVDD Gradient of TC11 Curves 96~103.5°C • THGVD [5:0]: Set temperature hysteresis value <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>THGVD [5:0]</th> <th>temperature hysteresis value</th> </tr> </thead> <tbody> <tr> <td>000000</td> <td>0 °C</td> </tr> <tr> <td>000001</td> <td>0.5 °C</td> </tr> <tr> <td>000010</td> <td>1.0 °C</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>111110</td> <td>31.0 °C</td> </tr> <tr> <td>111111</td> <td>31.5 °C</td> </tr> </tbody> </table>												THGVD [5:0]	temperature hysteresis value	000000	0 °C	000001	0.5 °C	000010	1.0 °C	:	:	111110	31.0 °C	111111	31.5 °C
THGVD [5:0]	temperature hysteresis value																									
000000	0 °C																									
000001	0.5 °C																									
000010	1.0 °C																									
:	:																									
111110	31.0 °C																									
111111	31.5 °C																									



7.2.65 Set GVCL Temperature Compensation Gradient Curves1

C4H	Set GVCL Temperature Compensation Gradient Curves1											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SETTCGVD1	0	1	↑	1	1	0	0	0	1	0	0	C4
1st parameter	1	1	↑	MTGVC1[3:0]				MTGVC0[3:0]				00
2nd parameter	1	1	↑	MTGVC3[3:0]				MTGVC2[3:0]				00
3rd parameter	1	1	↑	MTGVC5[3:0]				MTGVC4[3:0]				00
4th parameter	1	1	↑	MTGVC7[3:0]				MTGVC6[3:0]				00
Description	<ul style="list-style-type: none"> ▪ MTGVCx[3]: TCx(x=0~7) polarity 1: Positive, 0: Negative ▪ MTGVC0[2:0]: Set GVCL Gradient of TC0 Curves -40~-32°C ▪ MTGVC1[2:0]: Set GVCL Gradient of TC1 Curves -32~-24°C ▪ MTGVC2[2:0]: Set GVCL Gradient of TC2 Curves -24~-16°C ▪ MTGVC3[2:0]: Set GVCL Gradient of TC3 Curves -16~-8°C ▪ MTGVC4[2:0]: Set GVCL Gradient of TC4 Curves -8~0°C ▪ MTGVC5[2:0]: Set GVCL Gradient of TC5 Curves 0~8°C ▪ MTGVC6[2:0]: Set GVCL Gradient of TC6 Curves 8~16°C ▪ MTGVC7[2:0]: Set GVCL Gradient of TC7 Curves 16~24°C 											

7.2.66 Set GVCL Temperature Compensation Gradient Curves2

C5H	Set GVCL Temperature Compensation Gradient Curves2											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SETTCGVD2	0	1	↑	1	1	0	0	0	1	0	1	C5
1st parameter	1	1	↑	MTGVC9[3:0]				MTGVC8[3:0]				00
2nd parameter	1	1	↑	MTGVCA[3:0]				MTGVCB[3:0]				00
3rd parameter	1	1	↑	MTGVCC[3:0]				MTGVCD[3:0]				00
4th parameter	1	1	↑	MTGVCE[3:0]				MTGVCF[3:0]				00
Description	<ul style="list-style-type: none"> ▪ MTGVCx[3]: TCx(x=8~F) polarity 1: Positive, 0: Negative ▪ MTGVC8[2:0]: Set GVCL Gradient of TC8 Curves 24~32°C ▪ MTGVC9[2:0]: Set GVCL Gradient of TC9 Curves 32~40°C ▪ MTGVCA[2:0]: Set GVCL Gradient of TCA Curves 40~48°C ▪ MTGVCA[2:0]: Set GVCL Gradient of TCA Curves 40~48°C ▪ MTGVCB[2:0]: Set GVCL Gradient of TCB Curves 48~56°C ▪ MTGVCC[2:0]: Set GVCL Gradient of TCC Curves 56~64°C ▪ MTGVCD[2:0]: Set GVCL Gradient of TCD Curves 64~72°C ▪ MTGVCE[2:0]: Set GVCL Gradient of TCE Curves 72~80°C ▪ MTGVCF[2:0]: Set GVCL Gradient of TCF Curves 80~88°C 											



7.2.67 Set GVCL Temperature Compensation Gradient Curves3

C6H	Set GVCL Temperature Compensation Gradient Curves3											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
SETTCGVD3	0	1	↑	1	1	0	0	0	1	1	0	C6
1st parameter	1	1	↑	MTGVC11[3:0]				MTGVC10[3:0]				00
2nd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
3rd parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
4th parameter	1	1	↑	1	0	1	0	0	1	0	1	A5
Description	<ul style="list-style-type: none"> ▪ MTGVCx[3]: TCx(x=10~11) polarity 1: Positive, 0: Negative ▪ MTGVC10[2:0]: Set GVCL Gradient of TC10 Curves 88~96°C ▪ MTGVC11[2:0]: Set GVCL Gradient of TC11 Curves 96~103.5°C 											

7.2.68 Set TC VGH Flag

C7H	Set TC VGH Flag																									
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX														
SETTCVGH	0	1	↑	1	1	0	0	0	1	1	1	C7														
1st parameter	1	1	↑	TAVGH[7:0]								00														
2nd parameter	1	1	↑	TBVGH[7:0]								00														
3rd parameter	1	1	↑	TCVGH[7:0]								00														
4th parameter	1	1	↑	0	0	0	0	THVGH[3:0]				00														
Description	<ul style="list-style-type: none"> ▪ TAVGH[7:0]: set the TC zone boundary between zone A and B ▪ TBVGH[7:0]: set the TC zone boundary between zone B and C ▪ TCVGH[7:0]: set the TC zone boundary between zone C and D ▪ THVGH [3:0]: Set temperature hysteresis value ▪ TxVGH=TxVGH[7:0] - 40(°C) <table border="1" style="margin-left: 40px;"> <thead> <tr> <th>THVGH [3:0]</th> <th>temperature hysteresis value</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>0 °C</td> </tr> <tr> <td>0001</td> <td>1 °C</td> </tr> <tr> <td>0010</td> <td>2 °C</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>1110</td> <td>14 °C</td> </tr> <tr> <td>1111</td> <td>15 °C</td> </tr> </tbody> </table>												THVGH [3:0]	temperature hysteresis value	0000	0 °C	0001	1 °C	0010	2 °C	:	:	1110	14 °C	1111	15 °C
THVGH [3:0]	temperature hysteresis value																									
0000	0 °C																									
0001	1 °C																									
0010	2 °C																									
:	:																									
1110	14 °C																									
1111	15 °C																									



7.2.69 Set TC VCOM Flag

C8H	Set TC VCOM Flag																									
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX														
SETTCVCOM	0	1	↑	1	1	0	0	1	0	0	0	C8														
1st parameter	1	1	↑	TAVCOM[7:0]								00														
2nd parameter	1	1	↑	TBVCOM[7:0]								00														
3rd parameter	1	1	↑	TCVCOM[7:0]								00														
4th parameter	1	1	↑	0	0	0	0	THVCOM[3:0]				00														
Description	<ul style="list-style-type: none"> ▪ TAVCOM [7:0]: set the TC zone boundary between zone A and B ▪ TBVCOM [7:0]: set the TC zone boundary between zone B and C ▪ TCVCOM [7:0]: set the TC zone boundary between zone C and D ▪ THVCOM [3:0]: Set temperature hysteresis value ▪ TxVCOM=TxVGH[7:0] – 40(°C) <table border="1" data-bbox="550 779 1233 1084"> <thead> <tr> <th>THVCOM [3:0]</th> <th>temperature hysteresis value</th> </tr> </thead> <tbody> <tr> <td>0000</td> <td>0 °C</td> </tr> <tr> <td>0001</td> <td>1 °C</td> </tr> <tr> <td>0010</td> <td>2 °C</td> </tr> <tr> <td>:</td> <td>:</td> </tr> <tr> <td>1110</td> <td>14 °C</td> </tr> <tr> <td>1111</td> <td>15 °C</td> </tr> </tbody> </table>												THVCOM [3:0]	temperature hysteresis value	0000	0 °C	0001	1 °C	0010	2 °C	:	:	1110	14 °C	1111	15 °C
THVCOM [3:0]	temperature hysteresis value																									
0000	0 °C																									
0001	1 °C																									
0010	2 °C																									
:	:																									
1110	14 °C																									
1111	15 °C																									

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7.2.70 Charge Pump Setting

5AH	Charge Pump Setting											
Ins./Par.	A1	ERD	RWR	D7	D6	D5	D4	D3	D2	D1	D0	HEX
CPSET	0	1	↑	0	1	0	1	1	0	1	0	5A
1st parameter	1	↑	1	0	CP2[2:0]			0	CP1[2:0]			20
2nd parameter	1	↑	1	0	CP4[2:0]			0	CP3[2:0]			31
3rd parameter	1	↑	1	1	0	1	0	0	1	0	1	A5
4th parameter	1	↑	1	1	0	1	0	0	1	0	1	A5

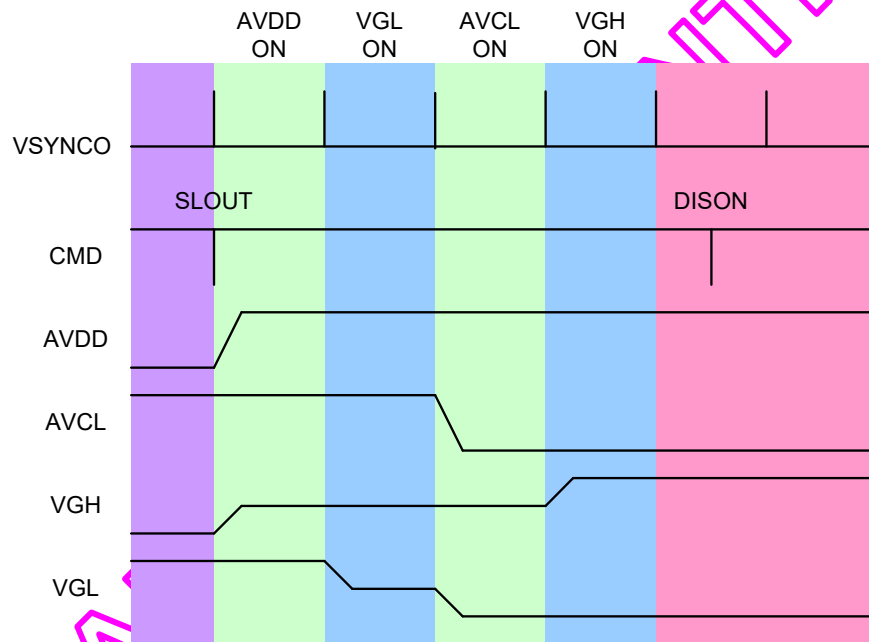
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Description

- CP1[2:0]: set AVDD power-on frame number after sleep out.
- CP2[2:0]: set AVCL power-on frame number after sleep out.
- CP3[2:0]: set VGL power-on frame number after sleep out.
- CP4[2:0]: set VGH power-on frame number after sleep out.

Default setting	Frame 0 (AVDD on)	Frame 1 (VGL on)	Frame 2 (AVCL on)	Frame 3 (VGH on)
AVDD (Voltage)	AVDD	AVDD	AVDD	AVDD
AVCL (Voltage)	0	0	AVCL	AVCL
VGH (Voltage)	AVDD	AVDD	AVDD	2VGHREG-VGL
VGL (Voltage)	0	nVGLREG	-3+nVGLREG	-3+nVGLREG

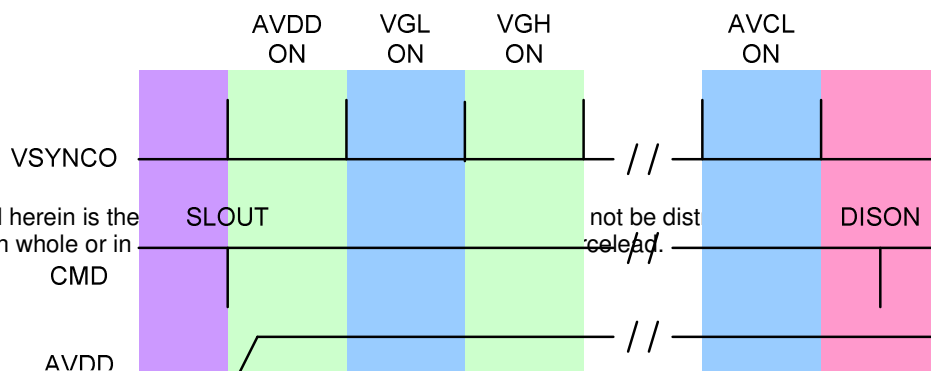


Default power on sequence of AVDD, AVCL, VGH, and VGL

Note:

1. If there is no Schottky Barrier Diode between VGL and AVCL, AVCL may be lower than VGL in some circumstances during power on. The power may not be stable in this situation.
2. We suggest a set of alternative power-on settings "CP1=0x00, CP2=0x07, CP3=0x01, CP4=0x02" to ensure power on smoothly.
3. Because the new setting of CP2 is larger than 4, please set PWRCTL(61h) FOFNo ≥ 4 simultaneously.

Recommended	Frame 0 (AVDD on)	Frame 1 (VGL on)	Frame 2 (VGH on)	Frame 7 (AVCL on)
AVDD (Voltage)	AVDD	AVDD	AVDD	AVDD
AVCL (Voltage)	0	0	0	AVCL
VGH (Voltage)	AVDD	AVDD	2VGHREG-VGL+3	2VGHREG-VGL
VGL (Voltage)	0	nVGLREG	nVGLREG	-3+nVGLREG



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celead.

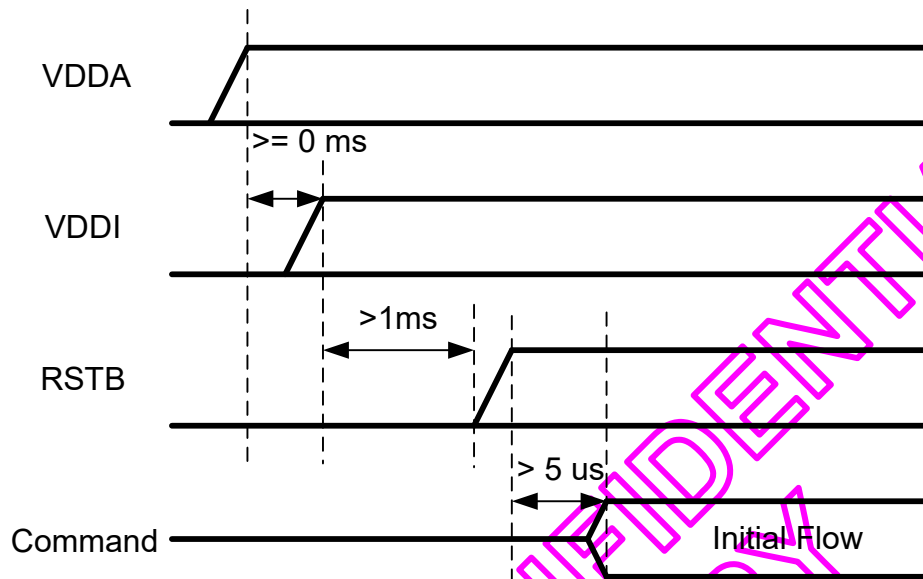


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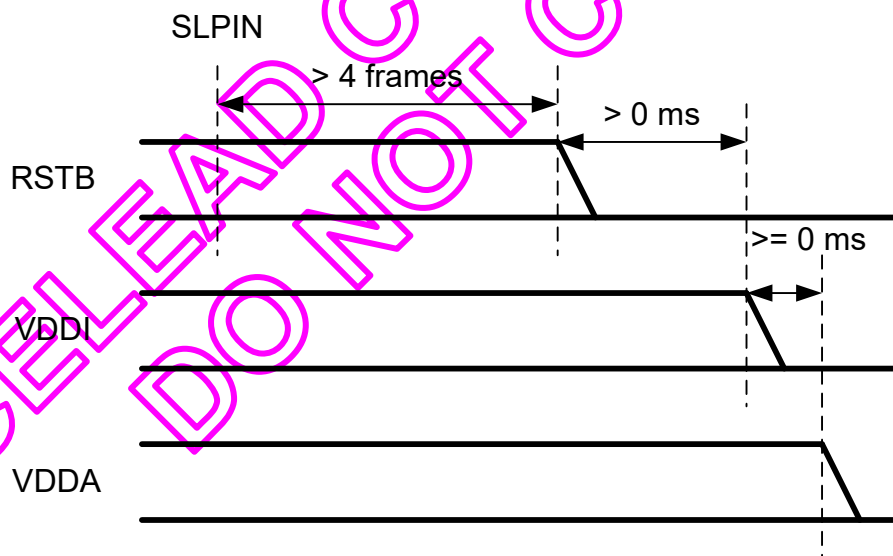


8. OPERATION FLOW

8.1 Power on/off Sequence



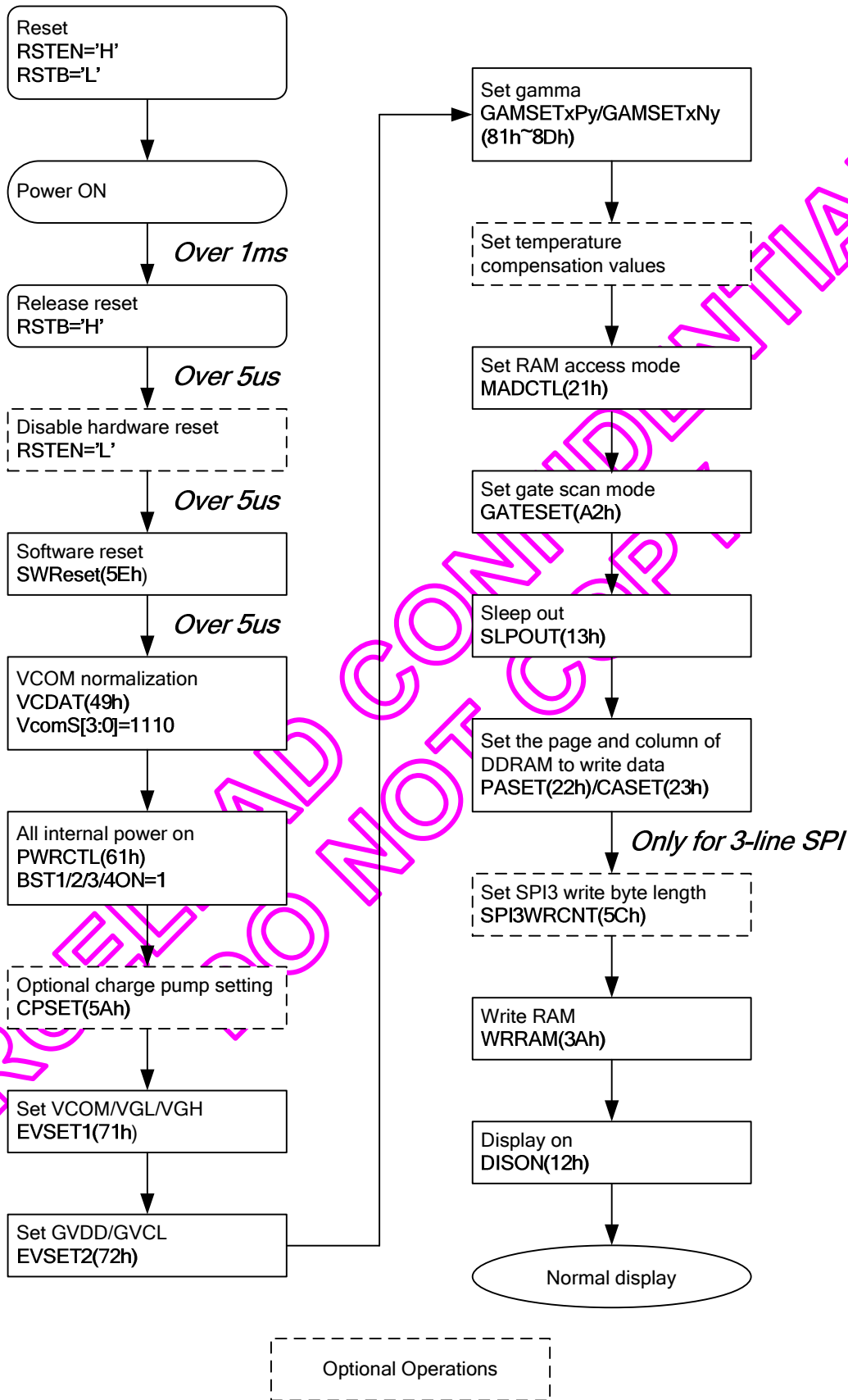
Power on sequence

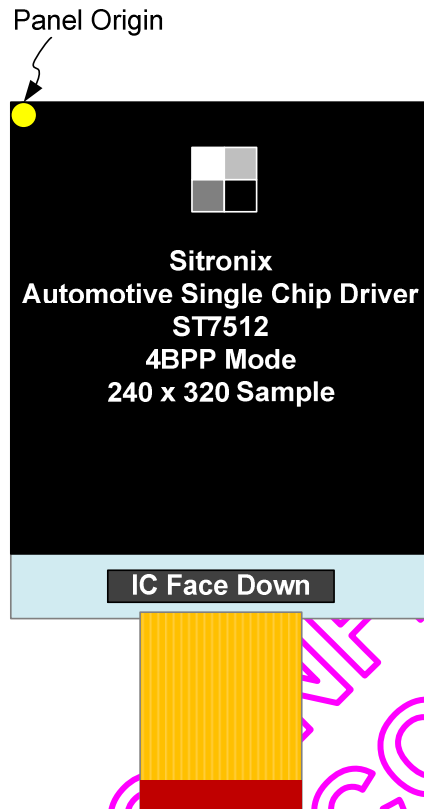


Power off sequence



8.2 Initial Flow



8.2.1 Reference Initial Code


```

void initial()
{
    Write( Command, 0x5E );           // SWRESET
    Write( Data, 0xA5 );
    Delay_ms(1);                     // Delay 1 ms

    Write( Command, 0x49 );           // Set VCOM Offset
    Write( Data, 0x0E );
    Write( Data, 0x00 );
    Write( Data, 0x00 );
    Write( Data, 0xA5 );

    Write( Command, 0x61 );           // Set Power Control
    Write( Data, 0x8F );               // n=2, all power on
    Write( Data, 0x44 );
    Write( Data, 0x02 );
    Write( Data, 0xA5 );

    Write( Command, 0x5A );           // Optional
    Write( Data, 0x70 );
    Write( Data, 0x21 );
    Write( Data, 0xA5 );
    
```



```
Write( Data, 0xA5);

Write( Command, 0x71 );           // Set Electronic Volume1
Write( Data, 0x1E );             // VCOM=-0.675V
Write( Data, 0x0B );            // VGH=15V
Write( Data, 0x0B );            // VGL=-10V
Write( Data, 0xA5 );

Write( Command, 0x72 );           // Set Electronic Volume2
Write( Data, 0x17 );             // GVDD=5.4V
Write( Data, 0x17 );            // GVCL=-5.4V
Write( Data, 0xA5 );
Write( Data, 0xA5 );

Write( Command, 0x81 );           // Set Gamma Positive1
Write( Data, 0x00 );
Write( Data, 0x16 );
Write( Data, 0x1B );
Write( Data, 0x1C );

Write( Command, 0x82 );           // Set Gamma Positive2
Write( Data, 0x1E );
Write( Data, 0x1F );
Write( Data, 0x20 );
Write( Data, 0x21 );

Write( Command, 0x83 );           // Set Gamma Positive3
Write( Data, 0x23 );
Write( Data, 0x24 );
Write( Data, 0x26 );
Write( Data, 0x28 );

Write( Command, 0x84 );           // Set Gamma Positive4
Write( Data, 0x2B );
Write( Data, 0x2F );
Write( Data, 0x34 );
Write( Data, 0x3F );

Write( Command, 0x89 );           // Set Gamma Negative1
Write( Data, 0x00 );
Write( Data, 0x16 );
Write( Data, 0x1B );
Write( Data, 0x1C );

Write( Command, 0x8A );           // Set Gamma Negative2
Write( Data, 0x1E );
```



```
Write( Data, 0x1F );
Write( Data, 0x20 );
Write( Data, 0x21 );

Write( Command, 0x8B );           // Set Gamma Negative3
Write( Data, 0x23 );
Write( Data, 0x24 );
Write( Data, 0x26 );
Write( Data, 0x28 );

Write( Command, 0x8C );           // Set Gamma Negative4
Write( Data, 0x2B );
Write( Data, 0x2F );
Write( Data, 0x34 );
Write( Data, 0x3F );

Write( Command, 0x21 );           // Set Memory Address Control
Write( Data, 0x01 );
Write( Data, 0xA5 );
Write( Data, 0xA5 );
Write( Data, 0xA5 );

Write( Command, 0x13 );           // Sleep out
Write( Data, 0xA5 );

Write( Command, 0x22 );           // Set Page Address
Write( Data, 0x00 );              // from page0
Write( Data, 0x9F );              // to page 159
Write( Data, 0x00 );
Write( Data, 0xA5 );

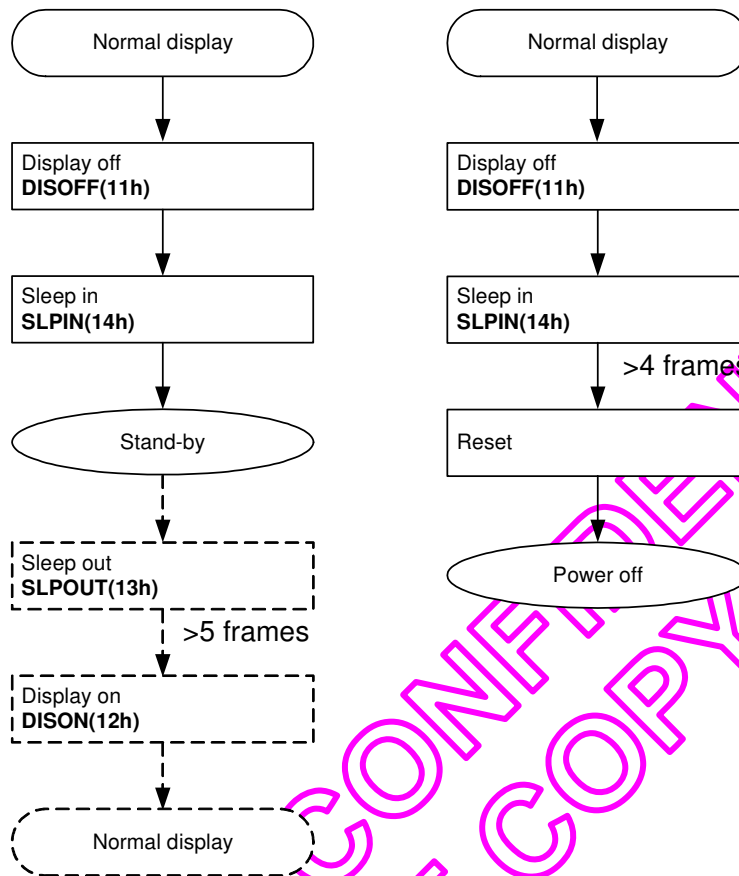
Write( Command, 0x23 );           // Set Column Address
Write( Data, 0x00 );              // from col0
Write( Data, 0x00 );
Write( Data, 0x00 );              // to col239
Write( Data, 0xEF );

Write( Command, 0x3A );           // Write DDRAM
Write( Data, 0xA5 );
for( int i = 0 ; i < 38400 ; i++ ) // Write 38400 bytes
Write( Data, 0x00 );              // Write black for the 1st pattern

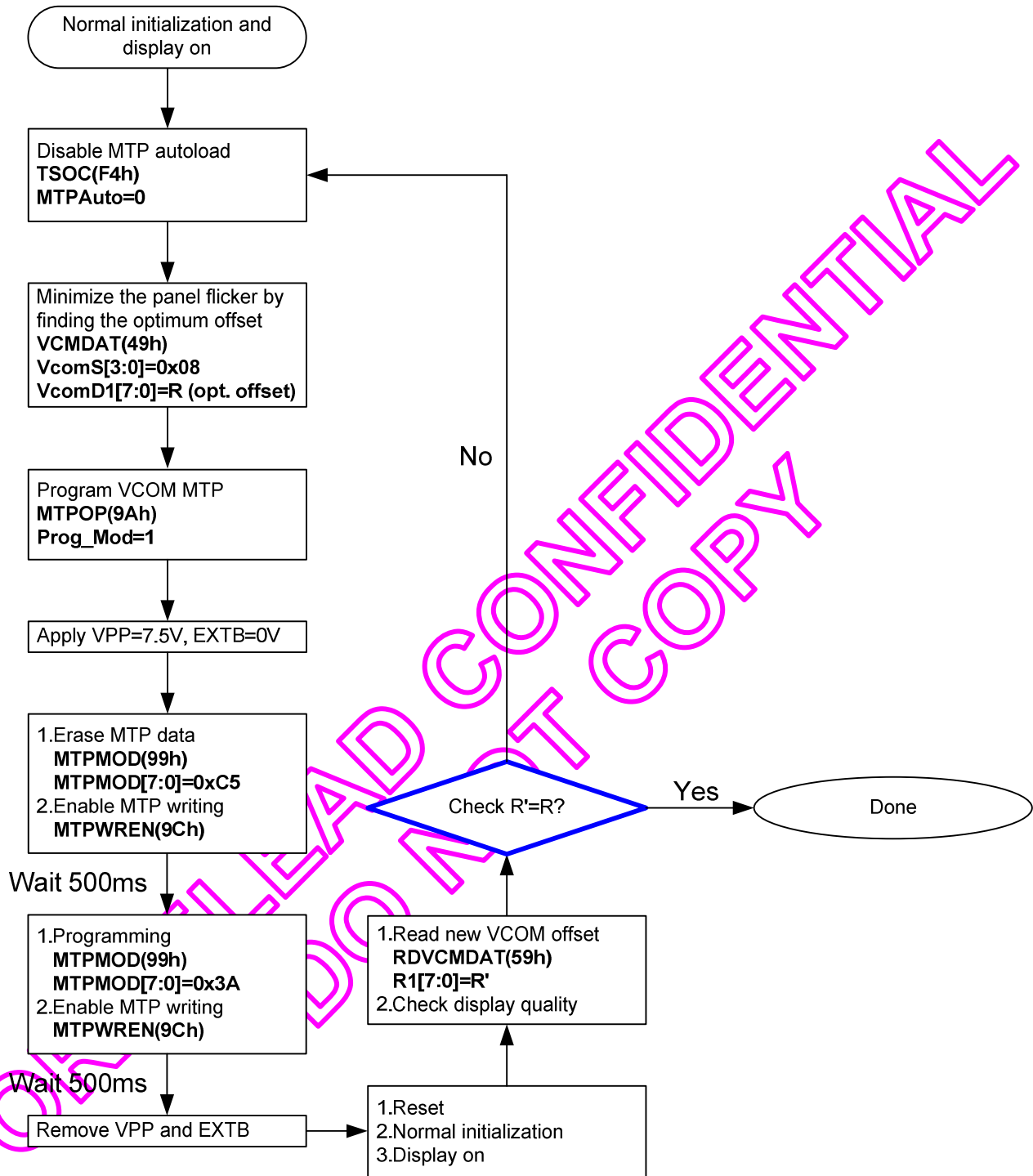
Write( Command, 0x12 );           // Display on
Write( Data, 0xA5 );
}
```



8.3 Stand-by and Power-off Flow



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8.4 MTP Flow for VCOM Offset


Note: The MTP can be written 3 times.



9. ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System; please refer to notes 1 and 2.

Parameter	Symbol	Conditions	Unit
I/O Power Supply Voltage	VDDI	-0.3 ~ 6.0	V
Analog Power supply voltage	VDDA	-0.3 ~ 6.5	V
Analog Power supply voltage	VDDP	-0.3 ~ 6.0	V
LCD Power supply voltage	AVDD, GVDD	7.0	V
	AVGL, GVGL, VCOM	-7.0	V
	VGH – VGL	35	V
MPU Interface Input Voltage	V _{IN}	-0.3 ~ VDDI+0.3	V
Operating temperature	TOPR	-40 ~ 105	°C
Storage temperature	TSTR	-55 ~ 120	°C

Notes:

1. Stresses exceed the absolute maximum ratings listed above may cause permanent damage to IC. The IC should be operated under the condition of DC/AC characteristics for normal operation. If this condition is not met, the IC may be malfunctioned, or the reliability may drop.
2. Parameters are valid in the operating temperature range unless otherwise specified. All voltages are with respect to VSS unless otherwise noted.

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10. DC CHARACTERISTICS

VSS = AGND = PGND = DGND = 0V; Temp = -40 ~ 105°C;

Item	Symbol	Condition	Rating			Unit	Applicable Pin
			Min.	Typ.	Max.		
Operating Voltage	VDDI	External Supply	2.7	—	5.5	V	VDDI
Operating Voltage	VDDA	External Supply	2.7	—	5.5	V	VDDA
Operating Voltage	VDDP	External Supply	2.7	—	5.5	V	VDDP
Operating Voltage	VCCO	Built-In Power Supply	—	1.8	—	V	VCCO
Operating Voltage	GVDD	Built-In Power Supply	2.7	—	5.8	V	GVDD
Operating Voltage	GVCL	Built-In Power Supply	-5.8	—	-2.7	V	GVCL
Operating Voltage	VGH	Built-In Power Supply	8.0	—	19.0	V	VGH
Operating Voltage	VGL	Built-In Power Supply	-15.0	—	-7.0	V	VGL
Operating Voltage	VCOM	Built-In Power Supply	-2	—	0	V	VCOM
Input High-level Voltage	V _{IH}		0.8 VDDI	—	VDDI	V	MPU Interface
Input Low-level Voltage	V _{IL}		VSS	—	0.2 VDDI	V	MPU Interface
Output High-level Voltage	V _{OH}	VDDI=2.7V, IOL=1mA	0.8 VDDI	—	VDDI	V	D[7:0]
Output Low-level Voltage	V _{OL}	VDDI=2.7V, IOL=1mA	VSS	—	0.2 VDDI	V	D[7:0]
Input Leakage Current	I _{LI}	V _{IN} =VDDI or DGND	-1.0	—	1.0	μA	MPU Interface
Output Voltage Deviation	ΔVS	Ta=25°C	—	±10	±20	mV	Source Pad
Read Temperature Offset	ΔT _{RD}	VDD=3.3V, Ta=25°C	—	-2	—	2	°C
		VDD=3.3V, Ta=-40~105°C	—	-4 *1	—	4 *1	

*1: Temperature accuracy is for reference only now. The target for all temperature range is ± 4°C and it is still under yield improvement stage.

The current consumed by whole IC (bare die) with internal power system:

Item	Symbol	Condition	Rating			Unit
			Min.	Typ.	Max.	
Display Current (Digital)	IDDI	VDDA=VDDP=VDDI=3.3V, Internal Power, 4bpp mode, Display ON	—	1	3	μA
Display Current (Analog)	IDDA + IDDP	Pattern: 1x1 Checker (Static), fFR= 60Hz Ta=-40~105°C		10,000	—	
Standby	ISS	VDDA=VDDP=VDDI=3.3V, Internal Power, Ta=-40~105°C	—	250	—	μA

Note: The current is DC characteristic of a "Bare Chip".



11. AC CHARACTERISTICS

11.1 Oscillation Frequency

AGND = PGND = DGND = 0V, VDDA = VDDP = VDDI = 3.0 ~ 5.0V, Ta = -40 ~ 105°C

Item	Symbol	Condition	Rating			Unit	Applicable Pin
			Min.	Typ.	Max.		
Oscillation Frequency	fosc	Built in oscillator circuit is used	900	1000	1100	KHz	CL
External Clock Input Frequency	fosci		900	1000	1100	KHz	CL

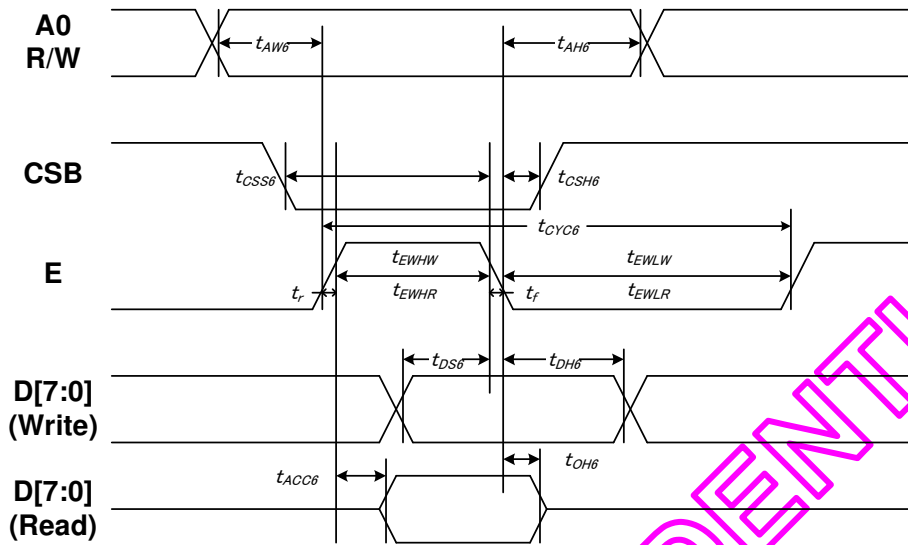
Note:

- External clock timing are specified based on the 20% and 80% of VDDI
- The rise and fall times (tr and tf) of the input signal are specified for less than 10ns.

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11.2 System Bus Timing for 6800 Series MPU



AGND = PGND = DGND = 0V, VDDA = VDDP = VDDI = 3.0 ~ 5.0V, Ta = -40 ~ 105°C

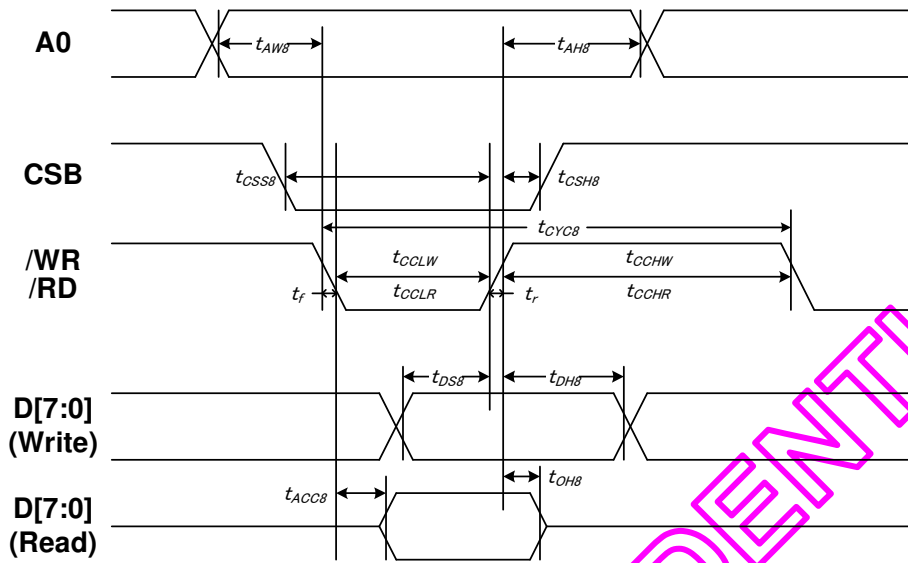
Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW6		10	—	ns
Address hold time		tAH6		0	—	
System cycle time	E	tCYC6		200	—	
Enable L pulse width (WRITE)		tEHLW		100	—	
Enable H pulse width (WRITE)		tEHWLW		100	—	
Enable L pulse width (READ)		tEHLR		130	—	
Enable H pulse width (READ)	tEHWLR		130	—		
CSB setup time	CSB	tCSS6		100	—	
CSB hold time		tCSH6		100	—	
Write data setup time	D[7:0]	tDS6		70	—	
Write data hold time		tDH6		20	—	
Read data access time	D[7:0]	tACC6	CL = 100 pF	—	80	
Read data output disable time		tOH6	CL = 100 pF	15	80	

Note:

- The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≤ (tCYC8 – tCCLR – tCCHR) are specified.
- All timing is specified using 20% and 80% of VDDI as the reference.
- tCCLW and tCCLR are specified as the overlap between CSB being “L” and /WR and /RD being at the “L” level. CSB and /WR (or /RD) cannot act at the same time and CSB should be 100ns wider than /WR (or /RD).



11.3 System Bus Timing for 8080 Series MPU



AGND = PGND = DGND = 0V, VDDA = VDDP = VDDI = 3.0 ~ 5.0V, Ta = -40 ~ 105°C

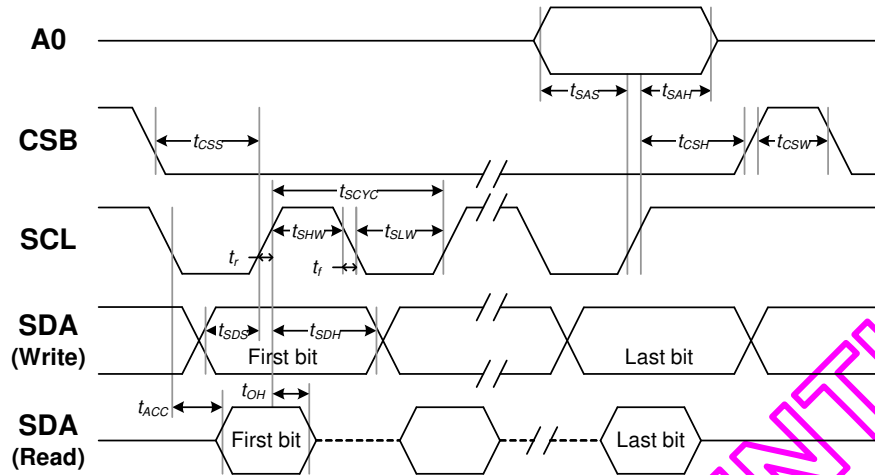
Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	tAW8		10	—	ns
Address hold time		tAH8		0	—	
System cycle time	/WR	tCYC8		200	—	
/WR L pulse width (WRITE)		tCCLW		100	—	
/WR H pulse width (WRITE)		tCCHW		100	—	
/RD L pulse width (READ)		tCCLR		120	—	
/RD H pulse width (READ)		tCCHR		120	—	
CSB setup time		CSB	tCSS8		100	
CSB hold time	tCSH8			100	—	
WRITE Data setup time	D[7:0]	tDS8		70	—	
WRITE Data hold time		tDH8		20	—	
READ access time		tACC8	CL = 100 pF	—	80	
READ Output disable time		tOH8	CL = 100 pF	15	80	

Note:

- The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, (tr + tf) ≤ (tCYC8 – tCCLW – tCCHW) for (tr + tf) ≤ (tCYC8 – tCCLR – tCCHR) are specified.
- All timing is specified using 20% and 80% of VDDI as the reference.
- tCCLW and tCCLR are specified as the overlap between CSB being “L” and /WR and /RD being at the “L” level. CSB and /WR (or /RD) cannot act at the same time and CSB should be 100ns wider than /WR (or /RD).



11.4 System Bus Timing for 4-Line Serial Interface



AGND = PGND = DGND = 0V, VDDA = VDDP = VDDI = 3.0 ~ 5.0V, Ta = -40 ~ 105°C

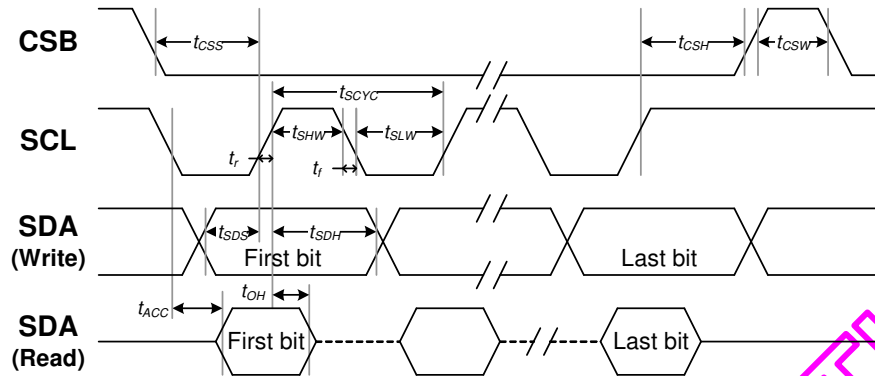
Item	Signal	Symbol	Condition	Min.	Max.	Unit
Address setup time	A0	t_{SAS}		32	—	ns
Address hold time		t_{SAH}		28	—	
Serial clock period (Write)	SCL	t_{SCYC}		60	—	
Serial clock period (Read)				110		
SCL "H" pulse width (Write)			t_{SHW}	28	—	
SCL "H" pulse width (Read)				40		
SCL "L" pulse width (Write)	SCL	t_{SLW}		32	—	
SCL "L" pulse width (Read)				70		
Write data setup time	SDA	t_{SDS}		15	—	
Write data hold time	(Write)	t_{SDH}		20	—	
Read data access time	SDA	t_{ACC}		—	80	
Read data output disable time	(Read)	t_{OH}		15	80	
CSB-SCL time	CSB	t_{CSS}		32	—	
CSB-SCL time		t_{CSH}		28	—	
CSB "H" pulse width		t_{CSW}		15	—	

Note:

1. The input signal rise and fall time (t_r , t_f) are specified at 15 ns or less.
2. All timing is specified using 20% and 80% of VDDI as the standard.



11.5 System Bus Timing for 3-Line Serial Interface



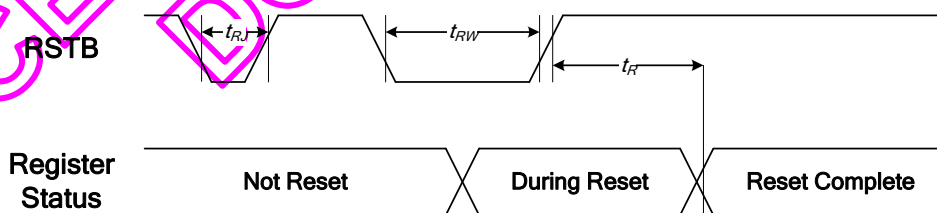
AGND = PGND = DGND = 0V, VDDA = VDDP = VDDI = 3.0 ~ 5.0V, -40 ~ 105°C

Item	Signal	Symbol	Condition	Min.	Max.	Unit	
Serial clock period (Write)	SCL	tSCYC		60	—	ns	
Serial clock period (Read)				110	—		
SCL "H" pulse width (Write)				tSHW	28		—
SCL "H" pulse width (Read)				tSHW	40		—
SCL "L" pulse width (Write)				tSLW	32		—
SCL "L" pulse width (Read)				tSLW	70		—
Write data setup time	SDA	tSDS		15	—		
Write data hold time	(Write)	tSDH		20	—		
Read data access time	SDA	tACC		—	80		
Read data output disable time	(Read)	tOH		15	80		
CSB-SCL time	CSB	tCSS		28	—		
CSB-SCL time		tCSH		32	—		
CSB "H" pulse width		tCSW		15	—		

Note:

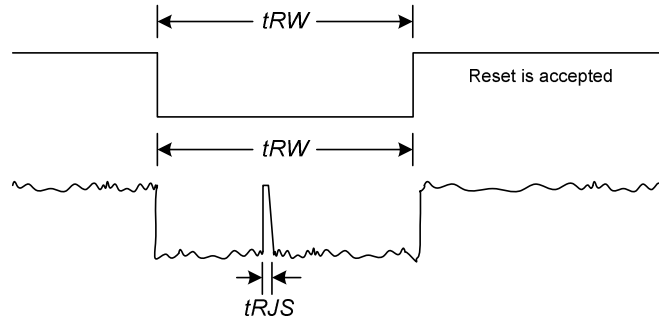
- The input signal rise and fall time (tr, tf) are specified at 15 ns or less.
- All timing is specified using 20% and 80% of VDDI as the standard.

11.6 Hardware Reset Timing



AGND = PGND = DGND = 0V, VDDA = VDDP = VDDI = 3.0 ~ 5.0V, Ta = -40 ~ 105°C

Item	Signal	Symbol	Condition	Rating		Unit
				Min.	Max.	
Reset time	RSTB	tR		—	5 ^{*1}	us
Reset "L" pulse width		tRW		15	—	
Reset rejection		tRJ		—	5	
Reset rejection (for noise spike)		tRJS		—	10	ns



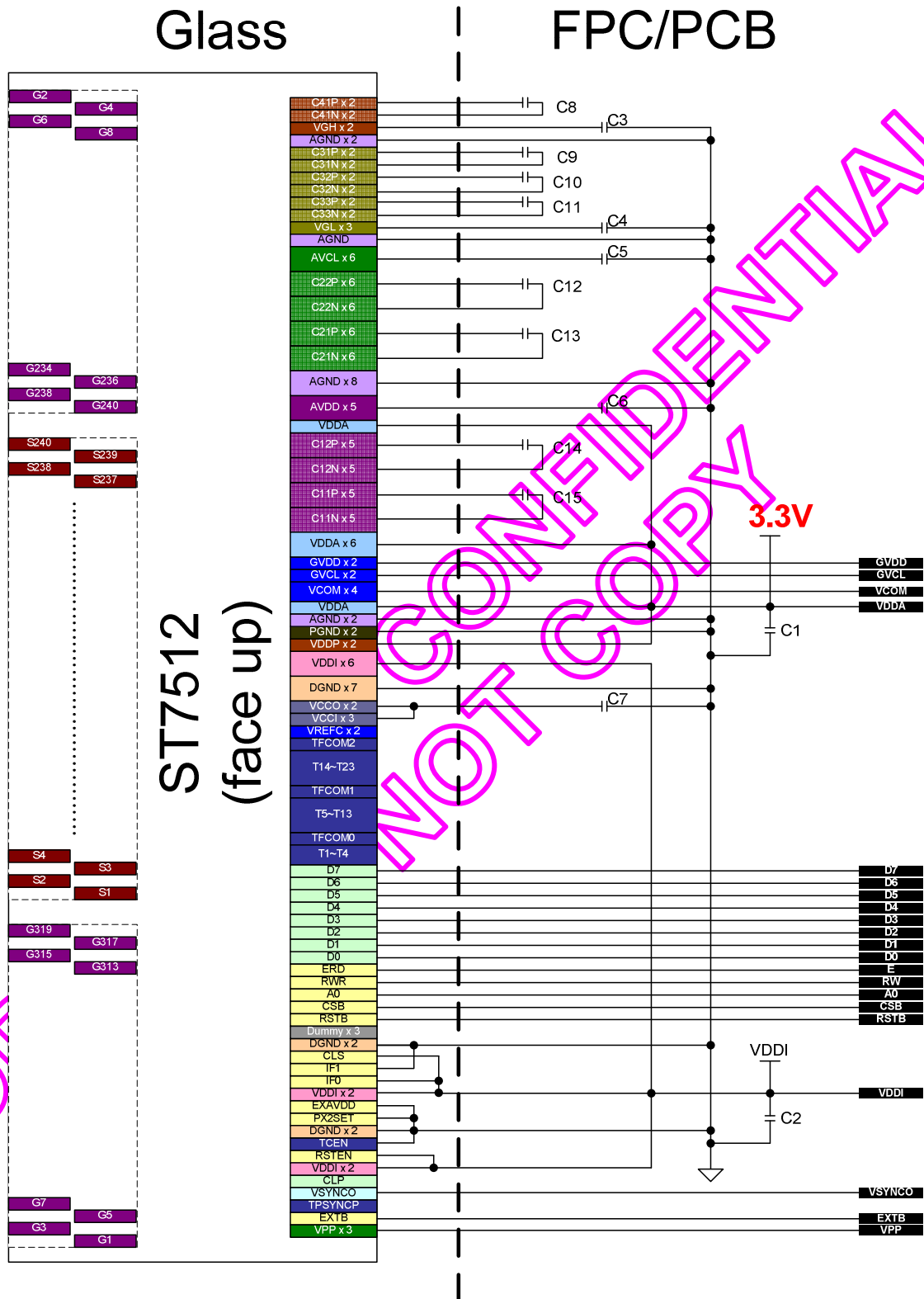
Note:

1. For PROM related operation, it takes 50ms at least for PROM Registers to load PROM contents. Do NOT use any PROM related command during this period.
2. When the system issues a RSTB LOW pulse, the reset procedure of IC will start if the LOW pulse is longer than t_{RW} specified above. If the LOW pulse is less than t_{RJS} specified above, the reset procedure of IC will not start. If the LOW pulse is longer than t_{RJS} and less than t_{RW} , the reset procedure of IC is not guaranteed.

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12. APPLICATION CIRCUIT

12.1 6800 Interface with VDDA=VDDP=3.3V

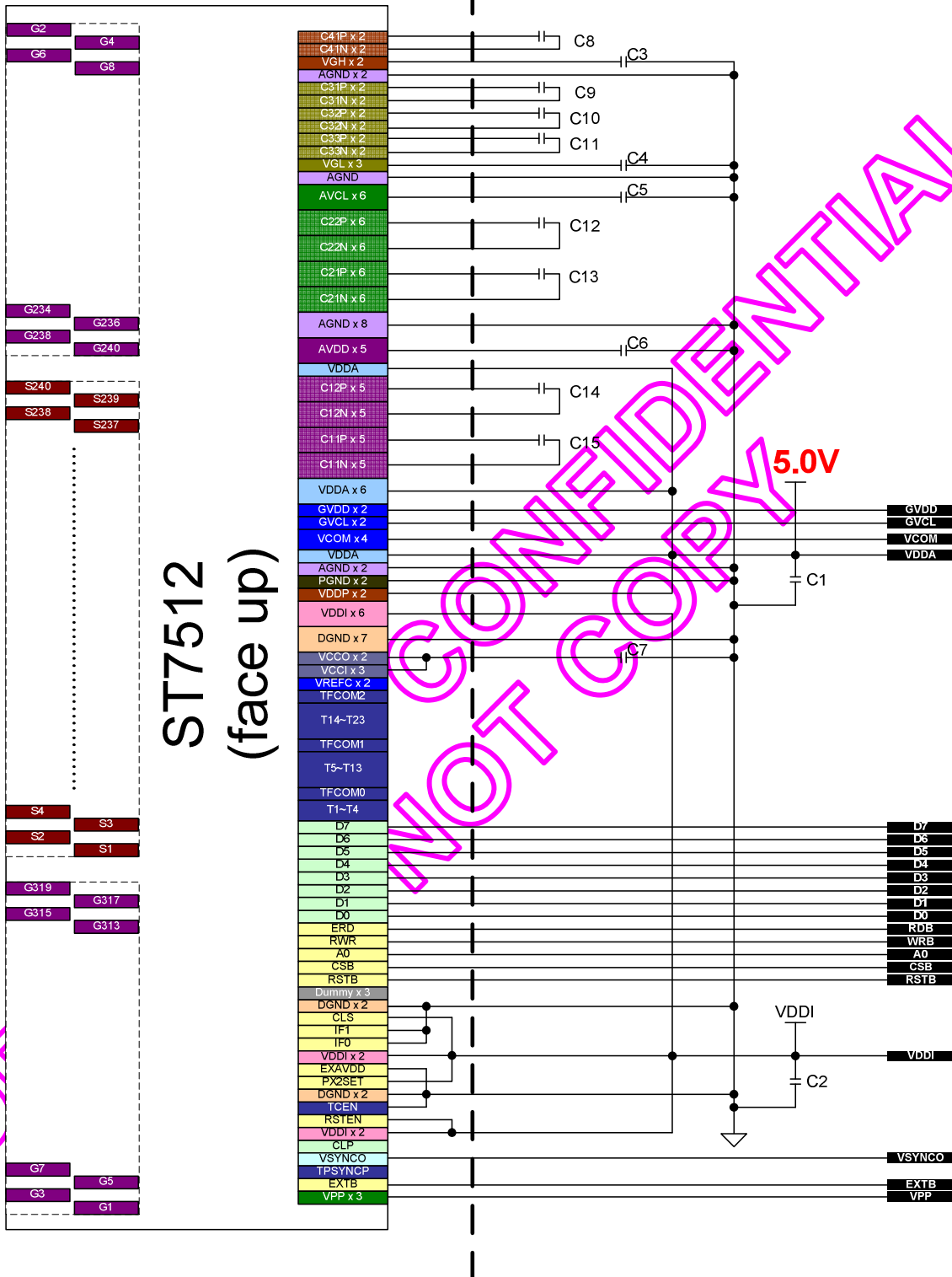




12.4 8080 Interface with VDDA=VDDP=5.0V

Glass

FPC/PCB



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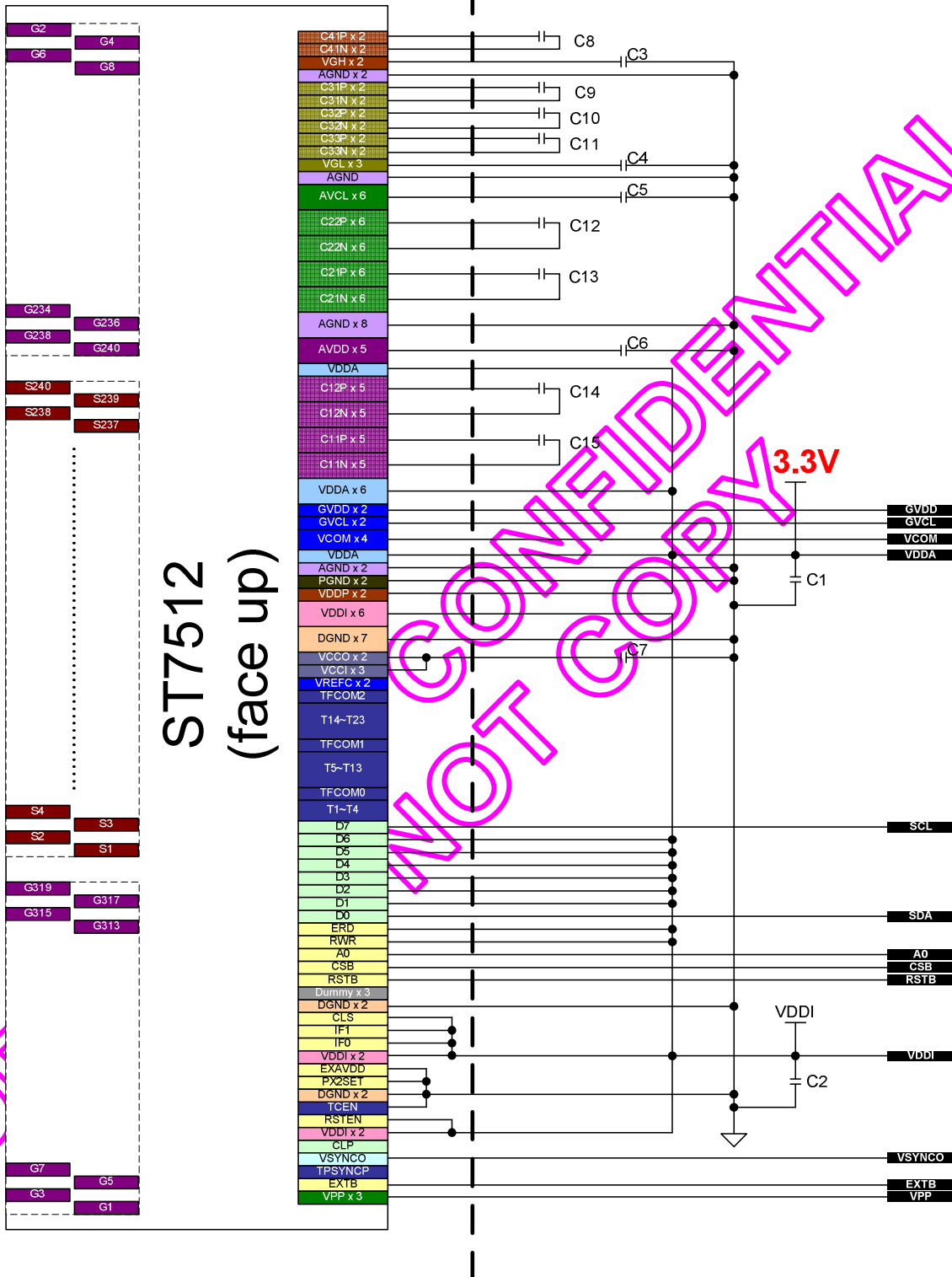
FOR



12.5 4SPI Interface with VDDA=VDDP=3.3V

Glass

FPC/PCB



ST7512
(face up)

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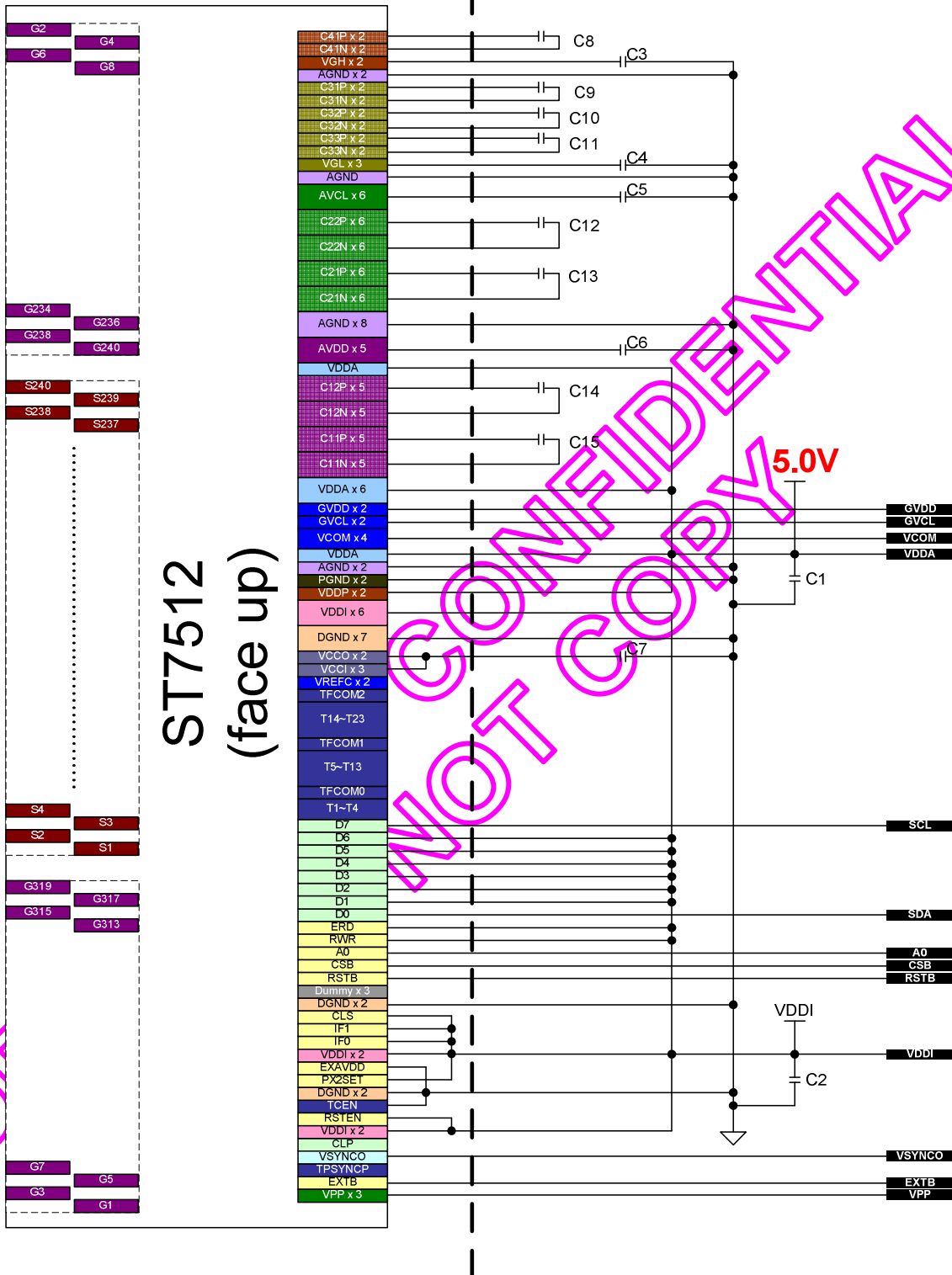
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12.6 4SPI Interface with VDDA=VDDP=5.0V

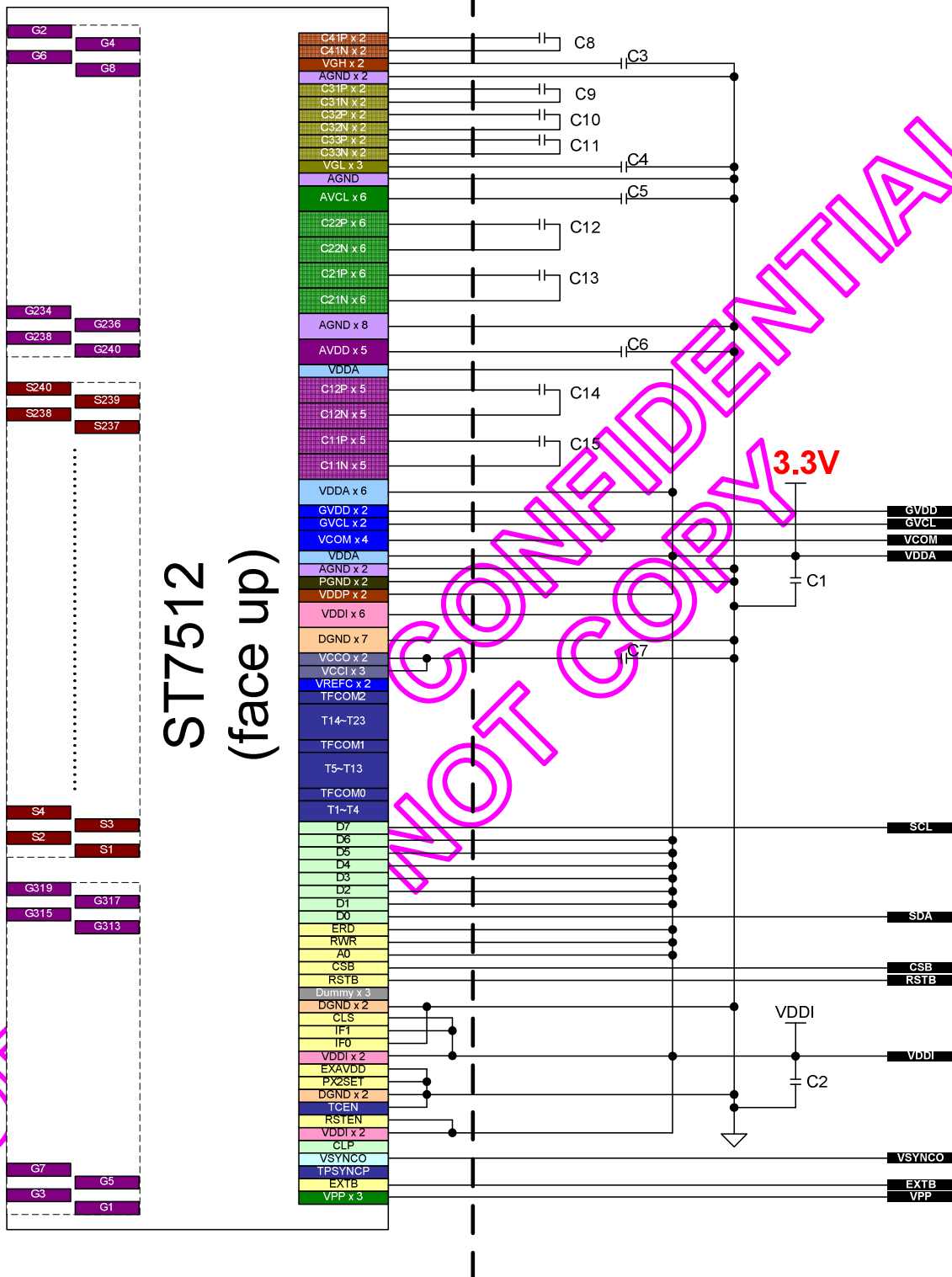
Glass

FPC/PCB



12.7 3SPI Interface with VDDA=VDDP=3.3V

Glass | FPC/PCB



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13. REVISION HISTORY

Version	Date	Description
2.0	2021/06	• Change format

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