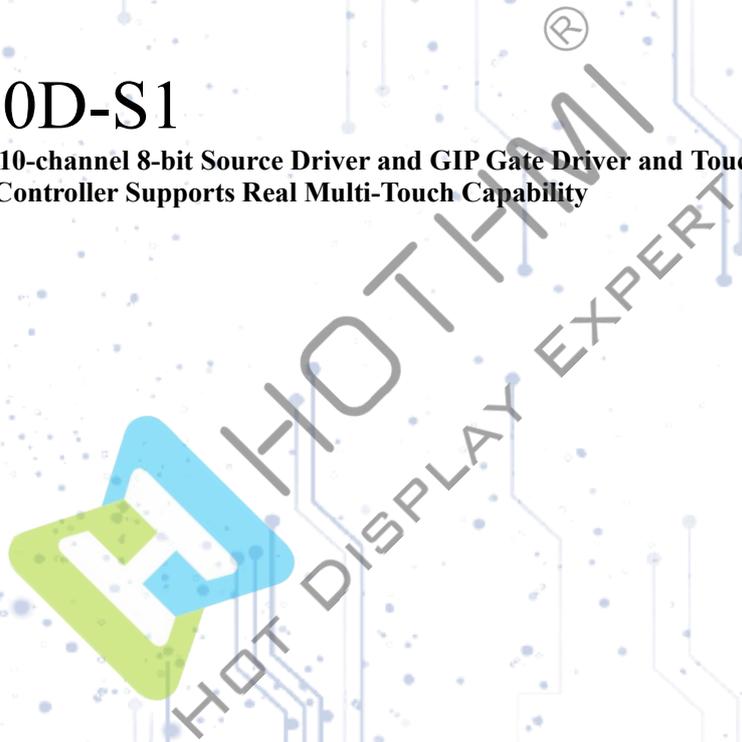


DATASHEET

AXS15260D-S1

In-Cell IC Integrates 810-channel 8-bit Source Driver and GIP Gate Driver and Touch Panel Controller Into a Single Chip with TP Controller Supports Real Multi-Touch Capability



Version V1.4
2025-06-27

AXS15260D-S1

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REVISION HISTORY

Date	Version	Description	Page	Author
2022/09/09	V0.0	draft	12	paulson
2023/01/05	V0.1	Preliminary version	179	Sand
2023/03/07	V0.2	improve all diagram	173	Sand
2023/04/24	V0.3	Improve diagram of MCU;Pad assignment	162	Sand
2023/05/09	V0.4	6.1 Absolute Operation Range	162	Sand
2023/07/12	V0.5	Update the VGH voltage;Update the display resolution information	162	Sand
2023/07/24	V0.6	Update the Power On/Off Sequence;Delete the 2 power mode	161	Sand
2023/08/26	V0.7	Update Note: VGH1:When the external on-load current is below 1.25mA, the maximum voltage can reach 16V, and the register can be adjusted normally; VGL1:When the external on-load current is below 1.35mA, the minimum voltage can reach -13V, and the register can be adjusted normally. Update the AC characteristic; Update the power Consumption. Add power block diagram Add power Supply Peripheral Component List	164	Sand
2023/10/12	V0.8	Update Block Diagram	169	AXS
2023/11/14	V0.9	Updated pin description for IM: the default /floating is 1.	169	Sand
2023/12/21	V1.0	Update PAD Assignment	169	AXS
2023/12/28	V1.1	1. Update PAD Assignment 2. Update application circuit 3. Update Logic Function Control(mipi BS)	169	AXS
2023/03/05	V1.2	1. Updated pin description 2. Delete SPI, QSPI, MCU image transmission interface 3. Update PAD Assignment:502~505 VCOM_OUT	-	Sand

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2024/06/07	V1.3	Update CSX Pin Description from output to input	-	Sand
2025/06/27	V1.4	Remove descriptions related to SPI, QSPI, and MCU interfaces	-	AXS



GENERAL DESCRIPTION

The AXS15260D-S1 highly integrates a-Si/LTPS TFT LCD driver and Super in-cell Touch controller, is a 16,777,216-color System-on-Chip (SOC) driver LSI designed for small and medium size TFT LCD display, and is capable of supporting up to 540RGBx1600(Dual gate) pixels in resolution. The 810-channel source driver can provide true 8-bit resolution and generate 256 Gamma-corrected values with an internal D/A converter.

The AXS15260D-S1 is able to operate with low IO interface power supply. Incorporating with several charge pumps, the AXS15260D-S1 can generate various voltage levels by an on-chip power management system for gate and source driver. Moreover, PWM for LED backlight, wake up-button enabling, respiratory lights and other functions, to provide customers with better experience.

In addition, the external Flash of AXS15260D-S1 can store not only the firmware used for Touch controller, but also the Initial code of LCD driver. After loading the initial code through the external Flash, the HOST only needs to send out "Sleep out" and "Display on" to turn on the LCD.

The built-in timing controller in the AXS15260D-S1 can support several functions to meet a wide variety of requirements for portable display applications. It provides several system interfaces, including MIPI/RGB, which can be used to configure the system. Furthermore, it can also archive high speed display data transmission by using the MIPI interface.



1 Features

1.1 Display

- ◆ One-chip solution for color amorphous a-Si TFT-LCD with incell
 - Display Resolution
 - Dual gate: 540RGB(up to 540,2 Columns/step) x 1600(up to 2048, 2 lines/step)
 - Single gate:270RGB(up to 270,2 Columns/step) x 1600(up to 2048,2 lines/step)
- ◆ Frame rate 60Hz/90Hz
- ◆ Support LTPS TFT-LCD:60Hz/90Hz,540RGB*1350
- ◆ Support IGZO TFT-LCD
- ◆ Display Data Memory: external PSRAM
- ◆ Support in-chip OTP
 - 2K*8 bit
 - OTP can stores trimming、ID1, ID2 (factory ID, 3bit) data
- ◆ System Interfaces
 - MIPI DSI (1/2/3/4 data lane,1.25Gbps/lane):
 - MIPI DSI (DSI v1.01.00, D-PHY v1.00.00 and DCS v1.01).
 - 16bit/18bit/24bit RGB(60Hz) interface
- ◆ Display Features
 - Colour depth 888, 666, 565
 - Analog gamma, 256 gray level
 - Support 8-color and 2-color mode
- ◆ On Chip Function
 - RAM-less driver with MIPI video mode
 - Column Inversion & Dot Inversion
 - Support loading FLASH to driver registers & TP registers
 - Support 0 Flash
 - Support SPR communication protocol
 - Support 810 source channel
 - Built-in 17 GOUT signals(CGOUTL1-L17,CGOUTR1-R17) on each side of the chip,providing directly the driver signals to the GIP circuit on the LCD panel
 - Built-in internal oscillator

1.2 Touch

- ◆ 8-bit embedded MCU
- ◆ 480 SX channels
- ◆ Support five-point detection
- ◆ Point reporting rate 60Hz(frame rate 60Hz)/Point reporting rate 90Hz(frame rate 90Hz)/Point reporting rate 120Hz(frame rate 60Hz)
- ◆ Super self-capacitance detection technology
- ◆ Support wake up gesture function
- ◆ Anti-RF interference

- ◆ Automatic frequency hopping
- ◆ Water proof
- ◆ I2C/SPI data communication interface
- ◆ Internal ESD detection
- ◆ Power saving mode
- ◆ VDDI_TP and VDDI supplied independently
- ◆ Center area $\leq 1.0\text{mm}$, edge $\leq 1.5\text{mm}@5\text{mm}$ copper column

1.3 Power

◆ Supply Voltage Range

3-power mode

- VSP: 4.5V~6.5V, typ : 5.5V
- VSN: -6.5V~-4.5V, typ: -5.5V
- VDDI: 1.65V ~ 1.95V typ: 1.8V or 2.8V~3.6V typ: 3.3V

◆ Output Voltage Range

- Gamma Positive Voltage Range: VGSP~VGMP ($\text{VGMP} \leq \text{VSP} - 0.3$)
VGMP: 2.55~5.7V
VGSP: 0.05~2.5V
- Gamma Negative Voltage Range: VGMN~VGSN ($\text{VGMN} \geq \text{VSN} + 0.3$)
VGMN: -5.7~-2.55V
VGSN: -2.15~1V
- Source Output Range: VGSP~VGMP
- Positive Gate Driver Output Voltage Level(VGH):
IGZO: VGH1 12~16V
LTPS: VGH2 6.5~10.7V
- Negative Gate Driver Output Voltage Level(VGL):
IGZO: VGL1 -13~-7.6V
LTPS: VGL2 -10~-6V
- Common Electrode Output Voltage Level(VCOM): -2.5V~0V (10mv/step)

Note:

VGH1: When the external on-load current is below 1.25mA, the maximum voltage can reach 16V, and the register can be adjusted normally;

VGL1: When the external on-load current is below 1.35mA, the minimum voltage can reach -13V, and the register can be adjusted normally.

1.4 Others

- ◆ ESD
 - HBM $\geq 2000\text{V}$
 - MM $\geq 200\text{V}$

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- Latch up $\geq\pm 100\text{mA}$
- ◆ COG Package



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(only one rstn-pin, shared by driver and touch). Whenever there is effective touch sensed on the touch screen, Touch controller will send data transfer request to the HOST via INT port, and complete the point report to the HOST. HOST can communicate with AXS15260D-S1 via I2C or SPI. HOST can also reset Touch controller through RSTN port.

◆ External Flash

External Flash, used to store the Firmware, and LCD initialization code, can be added into the Touch controller.

◆ Watchdog

Watchdog is used to ensure the stability of the chip when in operation

◆ Internal voltage regulator

Internal voltage regulator generates power supply, which is to provide power to logic circuit.

2.1.2 Touch Operation Mode

Touch controller has the following three operation modes:

◆ Normal operating mode

In this mode, Touch controller scans the screen, and detects the touch actions.

◆ Monitor Mode

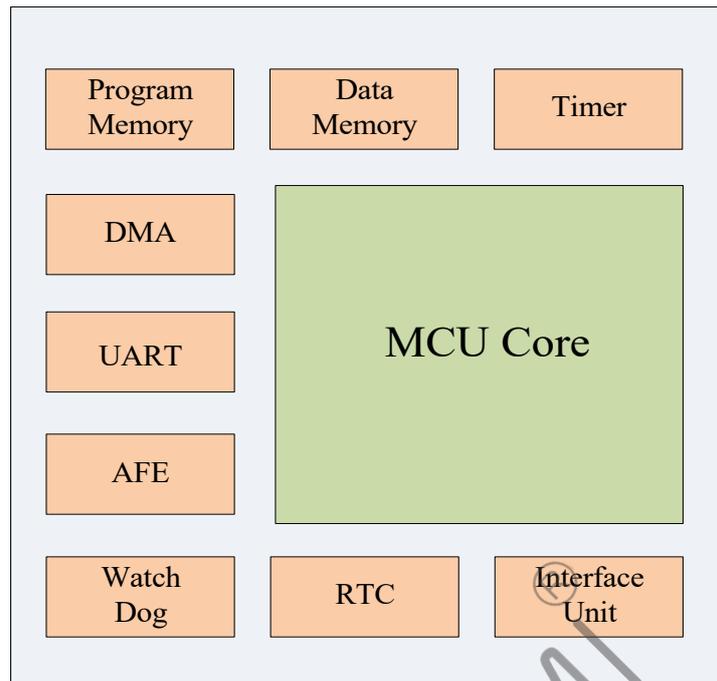
In this mode, Touch controller scans the screen intermittently to save power.

◆ Sleep mode

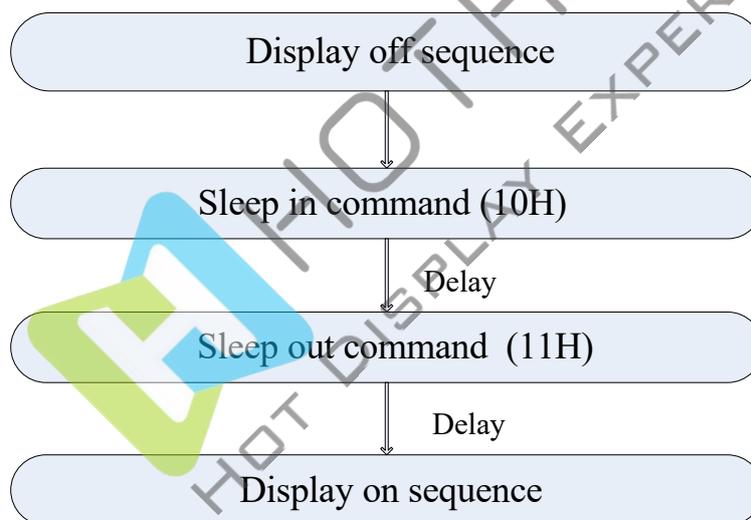
In this mode, Touch controller enters ultra low-power standby mode, HOST can only wake-up Touch controller via external signal to enter the normal operating mode. The power consumption in this mode is extremely small, and can greatly extend the standby time of mobile portable devices.

2.1.3 MCU

This section describes some critical features and operations supported by the MCU. The figure below shows the overall structure of the MCU block. In addition to the MCU core, we have added the following circuits.



2.1.4 Sleep In/Out Sequence



2.1.5 System interface

The AXS15260D-S1 supports the video data transmitted through the high-speed system interface, MIPI (Mobile Industry Processor Interface).

2.1.6 Grayscale voltage generating circuit

AXS15260D-S1 has true 8-bit resolution D/A converter, digital gamma cooperates with OP-AMP structure to enhance display quality. The grayscale voltage can be adjusted by grayscale data set in the γ -correction register and RGB can be adjusted separately.

2.1.7 Timing controller

AXS15260D-S1 has a timing controller, which can generate a timing signal for internal circuit

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operation such as gate output timing, image data accessing timing, etc.

2.1.8 Oscillator (OSC)

The AXS15260D-S1 has an internal oscillator to generate system clock.

2.1.9 Source driver circuit

AXS15260D-S1 consists of a 810-output source driver circuit.

2.1.10 Gate driver circuit

AXS15260D-S1 consists of a gate driver control circuit. The gate driver circuit outputs gate driver signals level at either VGH or VGL level.

2.1.11 LCD driving power supply circuit

The LCD driving power supply circuit generates the voltage levels VDD, VSP, VSN, VGH, VGL, VCOM for driving a LCD. All these voltages can be adjusted by register setting.

3 Pin Description

3.1 Power Supply and Regulator pins

PIN	I/O	Default value	Description
VDDI	I	Digital Power	External input voltage.1.8V power supply for digital interface
VDDI_DRV	I	Digital Power	External input voltage.1.8V power supply for digital interface
VDDI_FLH	I	Digital Power	External input voltage for external spi-flash
VDDI_HS	I	Digital Power	External input voltage for mipi-ldo
VDDI_PS	I/O	Digital Power	Psram IO power supply,connect VDDI when VDDI=1.8V, connect 1uF cap to gnd when VDDI=3.3V
VDDI_REF	I	Analog Power	Bandgap power supply
VDDI_TP	I	Digital Power	Power supply for TP digital interface.
VSN	I	Analog Power	-5.5V voltage power supply
VSNOUT	O	Analog Power	Charge pump output
VSP	I	Analog Power	5.5V voltage power supply
VSPOUT	O	Analog Power	Charge pump output,Connect VSP
VREF	O	Internal LDO	Output reference voltage.
VREF_PS	O	Internal LDO	Output reference voltage, need connect a stabilizing capacitor to VDDI_PS.
VREF_TP	O	Internal LDO	Regulator output voltage.
VGH	I	GIP power supply	GIP power supply connect VGHOUT1 or VGHOUT2
VGH_L	O	GIP power supply	Connect VGH
VGHO_L/R	O	GIP power supply	GIP power supply,VGHO_L connect to VGHO_R

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VGHO_REF	O	Charge pump	Connect a capacitor to VGHO_R
VGHOUT1	O	Charge pump	Charge pump output
VGHOUT2	O	Charge pump	Charge pump output
VGL	I	GIP power supply	Power supply need connect a stabilizing capacitor to ground.
VGLO_L/R	O	GIP power supply	GIP power supply, VGLO_L connect to VGLO_R
VGLO_REF	O	GIP power supply	Connect a capacitor to VGLO_L
VGLOUT1	O	Charge pump	Charge pump output
VGLOUT2	O	Charge pump	Charge pump output
VDD	O	Internal LDO	Digital power supply, need connect a stabilizing capacitor to ground.
VDD_HS	O	Internal LDO	MIPI lower power circuit power supply, connect to VDD on FPC.
VDD_OSC	O	osc power supply	Osc power supply, connect to VDD
VDD_PLL	O	Internal LDO	Regulator output voltage for PLL.
VDD_TP	O	Internal LDO	Regulator output voltage. FPC Connect together. Connect a capacitor for stabilization.
VDN	O	Digital Power	Internal LDO output
HS_LDO	O	Internal LDO	MIPI high speed circuit power supply, need connect a stabilizing capacitor to ground.
VCG_TP	O	Internal LDO	Regulator output voltage. FPC Connect together. Connect a capacitor for stabilization.
VCL	O	Internal LDO	LDO negative output.
VCOM	O	Analog	VCOM signal output for panel. Need connect a stabilizing capacitor to ground.
VPP	I	Digital Power	Power supply.
VDDA_VCOM	I	analog power	VCOM power supply, connect VDN.
VSS_HS	I	Ground	MIPI ground, connect to VSSD on FPC
VSS_OSC	I	Ground	OSC ground
VSSA	I	Ground	Analog ground
VSSA_REF	I	Ground	Bandgap ground
VSSD	I	Ground	Digital ground

3.2 Drive interface

PIN	I/O	Default value	Description
DB<23:0>	I/O	Digital (VDDI)	DB[23:0] input data of rgb interface.
HSYNC	I	Digital (VDDI)	Line synchronizing signal of rgb interface.
VSYNC	I	Digital (VDDI)	Frame synchronizing signal of rgb interface.
PCLK	I	Digital (VDDI)	pixel clock signal of rgb interface.

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DE	I	Digital (VDDI)	Data enable signal of rgb interface;
DIN_SDA_DUAL	I/O	Digital (VDDI)	The second data input pin in spi dual data lane of spi slave.
DIN_SDA	I	Digital (VDDI)	The bidirectional data pin of SPI slave
SCL	I	Digital (VDDI)	Synchronous clock signal in SPI slave.
RS	I	Digital (VDDI)	command or parameter selection in spi 4wire 8bits.
CSX	I	Digital (VDDI)	Chip select input pin ("Low" enable) in SPI slave
SWIRE	O	Digital (VDDI)	Swire protocol setting pin (Note: "H" = VDDI level, "L" = VSSI level.)Output load 50pf.
TE	O	Digital (VDDI)	Output tearing effect signal from IC to phone,Default output hiz.
RSTN_DRV	I	Digital (VDDI)	Global reset, low active.

3.3 TP interface

PIN	I/O	Default value	Description
SX[480:1]	I/O	Analog	Separate COM Electrode(TP sensor PAD)
VCOM_PASS_L/R	I/O	Analog	Pass line for VCOM from ILB to OLB
RSTN_TP	I	Digital (VDDI_TP)	Reset, low active, weak pull up
WORK_MODE	I	Digital (VDDI_TP)	Selection of work interface;1:I2C , 0:spi; pull down
CSN_TP	I	Digital (VDDI_TP)	When WORK_MODE =1 , floating; when WORK_MODE =0, connect to phone spi interface chip selection signal, low active.
SCK_TP	I	Digital (VDDI_TP)	When WORK_MODE =1 , connect to phone i2c slave interface clock signal , need open drain and extern pull up. when WORK_MODE =0, connect to phone spi interface clock signal.

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MISO_TP	O	Digital (VDDI_TP)	Connect to phone spi interface data output signal, from SCK negative edge to MISO output need 6ns delay in digital internal, detail as followed spi timing. (phone input ,chip output, chip is spi_slv)
MOSI_TP	I/O	Digital (VDDI_TP)	Connect to phone I2C slave interface data input/output, need open drain and extern pull up. (chip is i2c_mst). connect to phone spi interface data input signal.(phone output ,chip input, chip is spi_slv)
CSN_FLH	O	Digital (VDDI_FLH)	Chip select of flash, low active, individual power for spi flash interface.Master output.
SCK_FLH	O	Digital (VDDI_FLH)	Clock output to flash, individual power for spi flash interface.
MISO_FLH	I	Digital (VDDI_FLH)	Data input from flash; need weak pull up to avoid floating, flash data output need 7ns delay from clock negative edge, individual power for spi flash interface.
MOSI_FLH	O	Digital (VDDI_FLH)	Data output to flash, individual power for spi flash interface.

3.4 MIPI Interface

PIN	I/O	Default value	Description
HS_CN	I	MIPI	MIPI-DSI clock Lane positive-end/ negative-end input pin. These pins are MIPI-DSI CLK+/- differential clock signals if MIPI interface is used.HS_CP/N are differential small amplitude signals. Ensure the trace length is shortest ,so that the COG resistance is less than 10 ohm.If not used, please connect these pins to VSSAM.
HS_CP			
HS_D0N	I/O	MIPI	MIPI-DSI data Lane 0 positive-end/ negative-end pin. These pins are MIPI-DSI D0+/- differential data signals if MIPI interface is used.HS_D0P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. If not used, please connect these pins to VSSAM.
HS_D0P			
HS_D1N	I	MIPI	MIPI-DSI data Lane 1 positive-end/ negative-end input pin. These pins are MIPI-DSI D1+/- differential data signals if MIPI interface is used.HS_D1P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. If not used, please connect these pins to VSSAM.
HS_D1P			
HS_D2N	I	MIPI	MIPI-DSI data Lane 2 positive-end input pin. These pins are MIPI-DSI D2+/- differential data signals if MIPI interface is used.HS_D2P/N are differential small amplitude signals. Ensure the trace length is shortest so that the COG resistance is less than 10 ohm. If not used, please connect these pins to VSSAM.
HS_D2P			
HS_D3N	I	MIPI	MIPI-DSI data Lane 3 positive-end input pin. These pins are MIPI-DSI D3+/- differential data signals if MIPI interface is used.HS_D3P/N are differential small amplitude signals. Ensure

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HS_D3P			the trace length is shortest so that the COG resistance is less than 10 ohm. If not used, please connect these pins to VSSAM.
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3.5 PSRAM interface

PIN	I/O	Default value	Description
PS_ADQ<7:0>	I/O	Digital (VDDI_PS)	Address/DQ bus [7:0]
PS_CEN	O	Digital (VDDI_PS)	Chip select,active low,when CE=1 chip is standby state
PS_CLKN/P	O	Digital (VDDI_PS)	Clock signals,they must always be complementary,even in standby
PS_DM	O	Digital (VDDI_PS)	Data mask,active high.DM=1 mens “do not write”
PS_DQS	I/O	Digital (VDDI_PS)	PSRAM DQ Strobe clock

3.6 Test/Dummy Signal/ Other

PIN	I/O	Default value	Description
AATEST0_NV	O	Analog (VSP/VSN)	Test pin
AATEST1_PV			
AATEST2_LV			
AATEST3_LV			
AATEST4_NV			
AATEST5_PV			
AATEST6_PV			
AATEST7_NV			
SWIRE	O	Digital (VDDI)	Swire protocol setting pin (Note: “H” = VDDI level, “L” = VSSI level.)Output load 50pf.
TE	O	Digital (VDDI)	Output tearing effect signal from IC to phone,Default output hiz.
TS_SEL	I	Digital (VDDI)	test pad

3.7 Panel driver Signals

PIN	I/O	Default value	Description
S[810:1]	O	Analog	Output source driver signals. The D/A converted 256-gray-scale analog voltage output.
CGOUT_L<17:1>	O	Analog (VGHO/VGLO)	Gate control signals for panel in left side of IC.

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CGOUT1_R<17:1>	O	Analog (VGHO/VGLO)	Gate control signals for panel in right side of IC.
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3.8 Logic Function Control

PIN	I/O	Default value	Description
OTP_EXT_EN	I	Digital	Conect VSP or floating.
IGZO_MOD	I	Digital (VDDI)	0:IGZO panel 1:normal panel
PMOD_SEL	I	Digital (VDDI)	power voltage set pin: 0:when VDDI=3.3v 1(floating):when VDDI=1.8v
PSW_ENN	I	Digital (VDDI)	1:Power switching function enable 0:Some I/O power supplies are fixed to VDDI
PSW_PRIO_SEL	I	Digital (VDDI)	Select PIN for some IO power supplies 0:VDDI_TP is preferred 1:VDDI_DRV is preferred
LED_PWM	O	Digital (VDDI)	Used to adjust the brightness of panel backlight.
IM<3:0>	I	Digital (VDDI)	External interface select, the default /floating is 1.
BS<3:0>	I	Digital (VDDI)	Polarity and order of MIPI selection, default 4'bXXX.

外部 连接 BS[0]	外部连 接 BS[3:1]	HS_D 3P	HS_D 3N	HS_D 0P	HS_D 0N	HS_C P	HS_C N	HS_D 1P	HS_D 1N	HS_D 2P	HS_D 2N
1	000	HS_D 2P	HS_D 2N	HS_D 3P	HS_D 3N	HS_C P	HS_C N	HS_D 1P	HS_D 1N	HS_D 0P	HS_D 0N
	001	HS_D 0P	HS_D 0N	HS_D 3P	HS_D 3N	HS_C P	HS_C N	HS_D 1P	HS_D 1N	HS_D 2P	HS_D 2N
	010	HS_D 3P	HS_D 3N	HS_D 2P	HS_D 2N	HS_C P	HS_C N	HS_D 0P	HS_D 0N	HS_D 1P	HS_D 1N
	011	HS_D 3P	HS_D 3N	HS_D 0P	HS_D 0N	HS_C P	HS_C N	HS_D 2P	HS_D 2N	HS_D 1P	HS_D 1N
	100	HS_D 2P	HS_D 2N	HS_D 3P	HS_D 3N	HS_C P	HS_C N	HS_D 0P	HS_D 0N	HS_D 1P	HS_D 1N
	101	HS_D 0P	HS_D 0N	HS_D 3P	HS_D 3N	HS_C P	HS_C N	HS_D 2P	HS_D 2N	HS_D 1P	HS_D 1N
	110	HS_D 3P	HS_D 3N	HS_D 2P	HS_D 2N	HS_C P	HS_C N	HS_D 1P	HS_D 1N	HS_D 0P	HS_D 0N
	111	HS_D 3P	HS_D 3N	HS_D 0P	HS_D 0N	HS_C P	HS_C N	HS_D 1P	HS_D 1N	HS_D 2P	HS_D 2N
0	000	HS_D 2N	HS_D 2P	HS_D 3N	HS_D 3P	HS_C N	HS_C P	HS_D 1N	HS_D 1P	HS_D 0N	HS_D 0P

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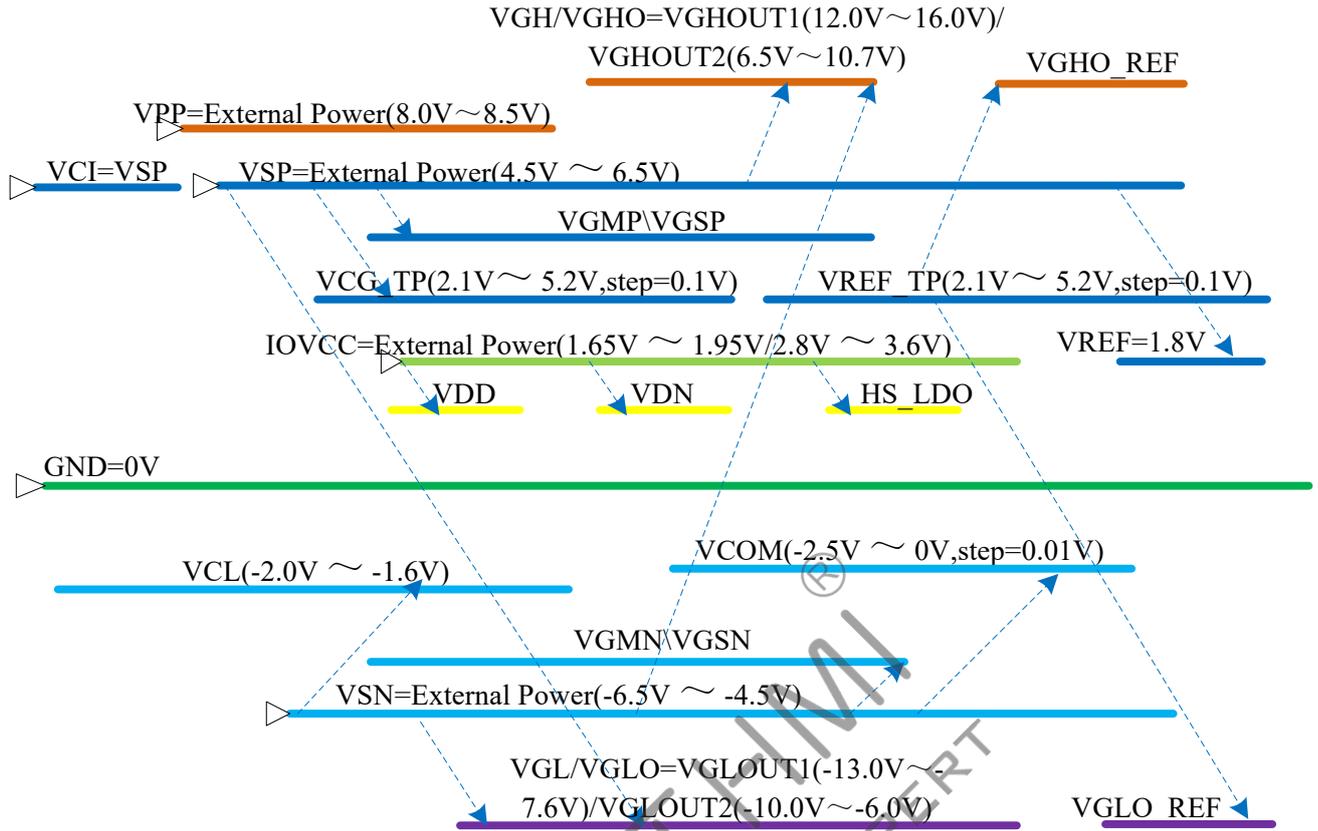
	001	HS _D 0N	HS _D 0P	HS _D 3N	HS _D 3P	HS _C N	HS _C P	HS _D 1N	HS _D 1P	HS _D 2N	HS _D 2P
	010	HS _D 3N	HS _D 3P	HS _D 2N	HS _D 2P	HS _C N	HS _C P	HS _D 0N	HS _D 0P	HS _D 1N	HS _D 1P
	011	HS _D 3N	HS _D 3P	HS _D 0N	HS _D 0P	HS _C N	HS _C P	HS _D 2N	HS _D 2P	HS _D 1N	HS _D 1P
	100	HS _D 2N	HS _D 2P	HS _D 3N	HS _D 3P	HS _C N	HS _C P	HS _D 0N	HS _D 0P	HS _D 1N	HS _D 1P
	101	HS _D 0N	HS _D 0P	HS _D 3N	HS _D 3P	HS _C N	HS _C P	HS _D 2N	HS _D 2P	HS _D 1N	HS _D 1P
	110	HS _D 3N	HS _D 3P	HS _D 2N	HS _D 2P	HS _C N	HS _C P	HS _D 1N	HS _D 1P	HS _D 0N	HS _D 0P
	111	HS _D 3N	HS _D 3P	HS _D 0N	HS _D 0P	HS _C N	HS _C P	HS _D 1N	HS _D 1P	HS _D 2N	HS _D 2P

IM[3:0]	Interface	Connect Pin
1111	MIPI	HS _{DN} ,HS _{DP} ,HS _{CN} ,HS _{CP} ,RSTN
1110	RGB 16/18/24-bit (Can be used with SPI 4wire)	DB[15/17/23:0],VSYNC_OSPI_DIN2,HSYNC,DE_QSPI_DIN3,P CLK,RSTN (DIN_SDA(MISO),DIN_SDA_DUAL(MOSI),RS(D/CX),SCL,CS X) ——The SPI interface can only support sending register instructions, not stream data

3.9 Power Block Diagram

The following is the power supply generation scheme, AXS1560A consists of VSP, VSN and IOVCC as the input power supply, and other power supply levels are generated in the chip.

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Note:

- 1.VDD include: VDD VDD_TP VDD_HS VDD_OSC
- 2.VDDI include: VDDI VDDI_DRV VDDI_FLH VDDI_HS VDDI_REF VDDI_TP VDDI_PS
- 3.VSS_HS=VSS_OSC=VSSA=VSSA_REF=VSSD=GND=0V

3.10 Power Supply Peripheral Component List

No.	NAME	Signal name	Values	Max ability	Note
1	C1	VCOM	4.7uF	10V	stabilizing capacitor
2	C2	VCG_TP	4.7uF	10V	stabilizing capacitor
3	C3	VDD	1uF	10V	stabilizing capacitor
4	C4	HS_LDO	1uF	10V	stabilizing capacitor
5	C5	VSP	4.7uF	10V	stabilizing capacitor
6	C6	VDDI	1uF	10V	stabilizing capacitor
7	C7	VSN	4.7uF	10V	stabilizing capacitor
8	C8	VGL	1.0uF	25V	stabilizing capacitor
9	C9	VGH	1.0uF	25V	stabilizing capacitor

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10	C10	VGHO_REF/VGHO	1uF	25V	stabilizing capacitor
11	C11	VGLO_REF/VGLO	1uF	25V	stabilizing capacitor
12	D1	VGL/VSN	-	-	
13	R1	IGZO_MOD/GND	0R	-	
14	R2	RSTN_DRV/RSTN_TP	0R	-	

4 INSTRUCTIONS

4.1 Outline

The AXS15260D-S1 supports high speed serial interface, MIPI, to configure the system via accessing command registers. While accessing the command registers, the information that indicates which register would be accessed should be sent first. After that, the new value can be updated via system interface. The MIPI-DSI is compliant with MIPI Alliance Standard for Display Serial Interface (DSI), Version 1.01.00 and D-PHY Version 1.00.00. Updating command instructions can also be accomplished by using all supporting system interfaces.

The AXS15260D-S1 has the following major categories of instructions:

- (1). User Command List and Description.
- (2). Manufacturer Command List and Description.

Since updating these instructions is asynchronous to the internal clock of the AXS15260D-S1, the updating procedure will require no waiting cycles. Furthermore, the updating procedure will not interfere with the processing of the host controller, this makes instructions can be handled smoothly and efficiently.

The following contents of this chapter will describe the supported instructions in detail.

4.2 User Command List and Description

4.2.1 Introduction

After the H/W reset by RESX pin or S/W reset by SWRESET command, each internal register will return to the default state. The commands 10h, 20h, 21h, 28h, 29h, 36h will be updated only during V-sync periods while the module is in the “Sleep Out” mode to avoid abnormal visual effects, and will be updated immediately in the “Sleep In” mode.

4.2.2 System Command List

Name	Hex	Write/Read Command	Description	Parameter Number	Transmission
NOP	00h	C	No operation	0	MIPI/ RGB
SWRESET	01h	C	Software reset	0	MIPI/ RGB
RDDID	04h	R	Read display	4	MIPI/ RGB
RDDNUMED	05h	R	Read Number of the Errors on DSI	1	MIPI/ RGB
RDDST	09h	R	Read display status	4	MIPI/ RGB
RDDPM	0Ah	R	Read display power	1	MIPI/ RGB
RDDMADCTL	0Bh	R	Read memory data access control	1	MIPI/ RGB

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RDDIPF	0Ch	R	Read Interface Pixel Format	1	MIPI/ RGB
RDDIM	0Dh	R	Read display image	1	MIPI/ RGB
RDDSM	0Eh	R	Read display signal	1	MIPI/ RGB
RDDSDR	0Fh	R	Read display self-diagnostic result	1	MIPI/ RGB
SLPIN	10h	C	Sleep in	0	MIPI/ RGB
SLPOUT	11h	C	Sleep out	0	MIPI/ RGB
PTLON	12h	C	Partial mode on	0	MIPI/ RGB
NORON	13h	C	Partial mode off(Normal)	0	MIPI/ RGB
INVOFF	20h	C	Display inversion off	0	MIPI/ RGB
INVON	21h	C	Display inversion on	0	MIPI/ RGB
DISPOFF	28h	C	Display off	0	MIPI/ RGB
DISPON	29h	C	Display on	0	MIPI/ RGB
CASET	2Ah	W	Column address set	4	MIPI/ RGB
RASET	2Bh	W	Row address set	4	MIPI/ RGB
PTLAR	30h	W	Partial start/end address set	4	MIPI/ RGB
PTLAR	31h	W	set_partial_columns	4	MIPI/ RGB
VSCRDEF	33h	W	Vertical scrolling definition	6	MIPI/ RGB
TEOFF	34h	C	Tearing effect line off	0	MIPI/ RGB
TEON	35h	W	Tearing effect line on	1	MIPI/ RGB
MADCTL	36h	W/R	Memory data access control	1	MIPI/ RGB
VSCRSADD	37h	W	Vertical scrolling start address	2	MIPI/ RGB
IDMOFF	38h	C	Idle mode off	0	MIPI/ RGB
IDMON	39h	C	Idle mode on	0	MIPI/ RGB
IPF	3Ah	W	Interface pixel format	1	MIPI/ RGB
TESCAN	44h	W	Set tear scanline	4	MIPI/ RGB
RDTESCAN	45h	R	Get tear scanline	4	MIPI/ RGB
WRDISBV	51h	W	Write display brightness value	1	MIPI/ RGB
RDDISBV	51h/52h	R	Read display brightness value	1	MIPI/ RGB
WRCTRLD	53h	W	Write display CTRL	1	MIPI/ RGB
RDCTRLD	54h	R	Read display CTRL	1	MIPI/ RGB

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			dsiplay		
RDFCHKSUM	Aah	R	Read First Checksum	2	MIPI/ RGB
RDCCHKSUM	Afh	R	Read Continue Checksum	2	MIPI/ RGB

4.2.2.1 User Command Description

4.2.2.1.1 SWRESET (01H): Software Reset

8'H01	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Description			Without parameters; Soft reset of the drv. If cr_soft_rstn_tp_opt=0, TP soft reset resets drv. If cr_soft_rstn_tp_opt=1, TP soft reset does not reset drv. When the TP register cr_soft_rstn_drv_opt=0, DRV soft reset can reset TP. When the TP register cr_soft_rstn_drv_opt=1, DRV soft reset non-resettable TP.								

4.2.2.1.2 ICI (04H): IC Information

8'HC0	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑	cr_manufacture_id								8'h00
Par1	-	↑	cr_driver_version_id								8'h00
Par2	-	↑	cr_driver_id								8'h00
Par3	-	↑	cr_id_dummy								8'h00
Description			cr_manufacture_id : the manufacture_id of the IC. cr_driver_version_id : the version_id of the IC. cr_driver_id : the IC id. cr_id_dummy : is cr_id_dummy_rev0,the dummy id0 that reserved. See the C0 command for details on the above registers.								

4.2.2.1.3 RDNUMED (05H): Read Number of the Errors on DSI

8'H05	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑	dsi_err_overflow	dsi_err_num							8'h00
Description			The first parameter is telling a number of the errors on DSI. When register cr_ecc_en=1, enable the mipi ecc function. When register cr_mipi_crc_en=1, the mipi crc function is enabled. dsi_err_num : ecc error number +crc error num dsi_err_overflow : dsi err num Indicates the overflow flag bit.								
			Readable error status (ECC and CRC)								

4.2.2.1.4 RDDST (09H): Read Display Status

8'H09	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
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Par0	-	↑	booster_en	cr_my	cr_mx			cr_bgr	cr_ca	cr_gs	8'h40
Par1	-	↑	rgb_format_new			idle_mode	cr_partial_en	pwr_on	normal_dsp_en		8'h70
Par2	-	↑	cr_vscroll_en		src_inv		dsp_on	tear_on			8'h00
Par3	-	↑			cr_tear_mode						8'h00
Description			<p>Read back command(21/20/36/10/11/28/29/3a)</p> <p>rgb_format_new: indicates the actual pixel format</p> <p>booster_en: charge pump Enables the booster function (vgh/vgl/vsp/vsn).</p> <p>idle_mode: 38/39h command flag. This bit is 1 when the 39h command is executed and 0 when the 38h command is executed.</p> <p>cr_partial_en: Part of the enable flag is displayed. The bit is 1 when the 12h command is executed and 0 when the 13h command is executed.</p> <p>normal_dsp_en: the opposite of cr_partial_en;</p> <p>pwr_on: indicates that the bit is 1 when the 11 command is executed, and the bit is 0 when the 10 command is executed.</p> <p>cr_vscroll_en: 33/37h Indicates that the running lamp function is enabled. 1 indicates that the running lamp function is enabled.</p> <p>src_inv: indicates the reverse flag bit of 0 and 1. If the flag bit is 1, the 21h command is executed. If the flag bit is 0, the 20 command is executed.</p> <p>dsp_on: indicates that the bit is 1 when the command is executed 29 and 0 when the command is executed 28.</p> <p>tear_on: This bit is set to 1 for issuing 35 and 0 for issuing 34.</p> <p>cr_tear_mode: 1 indicates that TE is H-blanking+V-blanking; 0 indicates that TE is V-blanking.</p>								

4.2.2.1.5 RDDMADCTL (0AH): Read Display MADCTL

8'H0A	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑	booster_en	idle_mode	cr_partial_en	pwr_on	normal_dsp_en	dsp_on	-	-	8'h00
Description			<p>booster_en: Enables the charge pump function.</p> <p>idle_mode: 38/39h command flag. This bit is 1 when the 39h command is executed and 0 when the 38h command is executed.</p> <p>pwr_on: indicates that the bit is 1 when the 11 command is executed, and the bit is 0 when the 10 command is executed.</p> <p>cr_partial_en: Part of the enable flag is displayed. The bit is 1 when the 12h command is executed and 0 when the 13h command is executed.</p> <p>normal_dsp_en: the opposite of cr_partial_en;</p> <p>dsp_on: indicates that the bit is 1 when the command is executed 29 and 0 when the command is executed 28.</p>								

4.2.2.1.6 RDDMADCTL (0BH): Read Display MADCTL

8'H0B	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑	cr_my	cr_mx			cr_bgr	cr_mh			8'h00
Description			Read back the parameters of command word 36h.								

4.2.2.1.7 RDDCOLMOD(0CH): Read Display Pixel Format

8'H0C	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑	0	dpi_format			0	dbi_format			8'h77
Description			Read back the parameters of command word 3Ah. dpi_format: video format rgb/mipi pixel format.								

4.2.2.1.8 RDDMADCTL (0DH): Read Display MADCTL

8'H0D	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑	cr_vsc roll_e n		src_in v						8'h00
Description			Read back 21/20h cr_vscroll_en: 33/37h Indicates that the running lamp function is enabled. 1 indicates that the running lamp function is enabled. src_inv: indicates the reverse flag bit of 0 and 1. If the flag bit is 1, the 21h command is executed. If the flag bit is 0, the 20 command is executed.								

4.2.2.1.9 RDDSM (0Eh): Read Display Signal Mode

8'H0E	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default																								
Par0	-	↑	tear_o n	cr_te ar_m ode	cr_h s fla g	cr_vs _flag	cr_pclk _flag	cr_de_f lag	0	dsi_err_e n	8'h00																								
Description			This command indicates the current status of the display as described in the table below:																																
			<table border="1"> <thead> <tr> <th>Bit</th> <th>Description</th> <th>Value</th> </tr> </thead> <tbody> <tr> <td>TEON</td> <td>Tearing effect line on/off</td> <td>'1' = ON, '0' = OFF,</td> </tr> <tr> <td>TEM</td> <td>Tearing effect line mode</td> <td>'1' = mode2, '0' = mode1,</td> </tr> <tr> <td>HS</td> <td>Horizontal Sync (RGB interface)</td> <td>'1' = ON, '0' = OFF,</td> </tr> <tr> <td>VS</td> <td>Vertical Sync (RGB interface)</td> <td>'1' = ON, '0' = OFF,</td> </tr> <tr> <td>PixelClk</td> <td>Pixel Clock (DOTCLK, RGB interface)</td> <td>'1' = ON, '0' = OFF,</td> </tr> <tr> <td>DataEn</td> <td>Data Enable (DE, RGB interface)</td> <td>'1' = ON, '0' = OFF,</td> </tr> <tr> <td>ErrorDSI</td> <td>Error On DSI (MIPI Interface)</td> <td>'1' = Error, '0' = No Error</td> </tr> </tbody> </table>									Bit	Description	Value	TEON	Tearing effect line on/off	'1' = ON, '0' = OFF,	TEM	Tearing effect line mode	'1' = mode2, '0' = mode1,	HS	Horizontal Sync (RGB interface)	'1' = ON, '0' = OFF,	VS	Vertical Sync (RGB interface)	'1' = ON, '0' = OFF,	PixelClk	Pixel Clock (DOTCLK, RGB interface)	'1' = ON, '0' = OFF,	DataEn	Data Enable (DE, RGB interface)	'1' = ON, '0' = OFF,	ErrorDSI	Error On DSI (MIPI Interface)	'1' = Error, '0' = No Error
Bit	Description	Value																																	
TEON	Tearing effect line on/off	'1' = ON, '0' = OFF,																																	
TEM	Tearing effect line mode	'1' = mode2, '0' = mode1,																																	
HS	Horizontal Sync (RGB interface)	'1' = ON, '0' = OFF,																																	
VS	Vertical Sync (RGB interface)	'1' = ON, '0' = OFF,																																	
PixelClk	Pixel Clock (DOTCLK, RGB interface)	'1' = ON, '0' = OFF,																																	
DataEn	Data Enable (DE, RGB interface)	'1' = ON, '0' = OFF,																																	
ErrorDSI	Error On DSI (MIPI Interface)	'1' = Error, '0' = No Error																																	

4.2.2.1.10 RDDSDR (0Fh): Read Display Self-Diagnostic Result

8'H0F	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par1	-	↑	otp_cr c_don e	ctn_crc _done	0			otp_crc_ ok		8'h00	
Description			This command indicates the current status of the display self-diagnostic result after sleep out command as described (test function) below: otp_crc_done: The otp is loaded and the crc check is complete ctn_crc_done: The host reconfigures the register and the crc check ends otp_crc_ok:otp Checksums Comparison, '0' = Checksums are same, '1' = Checksums are not same See sections: "Read First Checksum (Aah)" and "Read Continue Checksum (Afh)"								

4.2.2.1.11 POFF (10H): Power Off Command

8'H10	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Description			power off command(10) with no parameter is used to turn off power								

4.2.2.1.12 PON (11H): Power On Command

8'H11	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Description			power on command(11) with no parameter is used to turn on power								

4.2.2.1.13 PTLON (12H): Partial Display Mode On

8'H12	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Description			Without parameters; Enable the partial display function, that is, <code>cr_partial_en = 1</code> . The upper and lower boundary positions of the local display area are determined by the 30H command word. The left and right boundary of the local display area is determined by 31H command word. Local display area (within the boundary position) shows normal picture content; The contents of the non-local display area (outside the boundary position) are configured by registers (<code>cr_partial_value_r</code> , <code>cr_partial_value_g</code> , <code>cr_partial_value_b</code>).								

4.2.2.1.14 NORON (13H): Normal Display Mode On (Partial mode off)

8'H13	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Description			Without parameters; Disable the partial display function and switch to the normal display mode, that is, <code>cr_partial_en = 0</code> .								

4.2.2.1.15 NSI (20H): No Src_Inv Command

8'H20	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Description			no <code>src_inv</code> command(20) with no parameter is used to exit the inversion of black and white picture								

4.2.2.1.16 SI (21H): Src_Inv Command

8'H21	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Description			<code>src_inv</code> command(21) with no parameter is used to enter the inversion of black and white picture								

4.2.2.1.17 DOFF (28H): Display Off Command

8'H28	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Description			display off command(28) with no parameter is used to turn off display								

4.2.2.1.18 DON (29H): Display On Command

8'H29	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Description			display on command(29) with no parameter is used to turn on display								

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4.2.2.1.19 CWA (2AH): Column Windows Address Command

8'H2a	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default	
Par0	↑	-						cr_2a_sc_rx[10:8]			8'h00	
Par1	↑	-	cr_2a_sc_rx[7:0]									8'h00
Par2	↑	-						cr_2a_ec_rx[10:8]			8'h00	
Par3	↑	-	cr_2a_ec_rx[7:0]									8'h00
Description		When cr_win_en =1 of command table2, windowing functions 2a and 2b are effective; cr_2a_sc_rx: represent row/column start/stop address in command mode display cr_2a_ec_rx: represent row/column start/stop address in command mode display;										

4.2.2.1.20 RWA (2BH): Row Windows Address Command

8'H2b	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default	
Par0	↑	-						cr_2b_sr_rx[11:8]			8'h00	
Par1	↑	-	cr_2b_sr_rx[7:0]									8'h00
Par2	↑	-						cr_2b_er_rx[11:8]			8'h00	
Par3	↑	-	cr_2b_er_rx[7:0]									8'h00
Description		cr_2b_sr_rx: represent row/column start/stop address in command mode display; cr_2b_er_rx: represent row/column start/stop address in command mode display;										

4.2.2.1.21 PTLAR (30H):set_partial_rows

8'H30	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default	
Par0	↑	-						cr_partial_strow[11:8]			8'h00	
Par1	↑	-	cr_partial_strow[7:0]									8'h00
Par2	↑	-						cr_partial_endrow[11:8]			8'h00	
Par3	↑	-	cr_partial_endrow[7:0]									8'h00
Description		cr_partial_strow [11:0]: Locally displays the start row. cr_partial_endrow [11:0]: locally displays the endrow.										

4.2.2.1.22 PTLAR (31H):set_partial_columns

8'H31	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default	
Par0	↑	-						cr_partial_strcol[10:8]			8'h00	
Par1	↑	-	cr_partial_strcol[7:0]									8'h00
Par2	↑	-						cr_partial_endcol[10:8]			8'h00	
Par3	↑	-	cr_partial_endcol[7:0]									8'h00
Description		cr_partial_strcol [10:0]: locally displays the start column; cr_partial_endcol [10:0]: locally displays the end column.										

4.2.2.1.23 SA (33H): Scroll Area Command

8'H33	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
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Par0	↑	-	cr_33_tfa[15:8]	8'h00
Par1	↑	-	cr_33_tfa[7:0]	8'h00
Par2	↑	-	cr_33_vsa[15:8]	8'h00
Par3	↑	-	cr_33_vsa[7:0]	8'h00
Par4	↑	-	cr_33_bfa[15:8]	8'h00
Par5	↑	-	cr_33_bfa[7:0]	8'h00
Description		<p>If command table2 is cr_vscroll_en = 1, the running lamp function is effective. cr_33_tfa: indicates the top fix area. cr_33_vsa: vertical scroll area. cr_33_bfa: bottom fix area.</p>		

4.2.2.1.24 TEOFF (34H): Tearing Effect Line OFF

8'H34	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Description		Without parameters, Disables Tearing Effect output signal from TE signal line, i.e. tear_on = 0.									

4.2.2.1.25 TEON (35H): Tearing Effect Line On

8'H35	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	↑	-								cr_tear mode	8'h00
Description		Issue 35h, i.e. tear_on = 1, Tearing Effect Line On. TEM Determining the Tearing Effect Output Line mode. 1. TEM = 0: The Tearing Effect output line consists of V-Blanking information only. 2. TEM = 1: The Tearing Effect output Line consists of both V-Blanking and H-Blanking information. The TE of H-blanking is determined by C5 of command table2: cr_te_gspc: start column position; cr_te_gspf: indicates the end column position.									

4.2.2.1.26 DCTR (36H): Display Control Command

8'H36	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default																									
Par0	↑		MY	MX			BGR	MH	cr_ca	cr_gs	8'h00																									
Description		<p>cr_gs: gip scan direction setting.</p> <table border="1"> <thead> <tr> <th>cr_gs</th> <th>cr_fv</th> <th>result</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>FW, select D7 and D8 register groups</td> </tr> <tr> <td>0</td> <td>1</td> <td>BW, select D9 and DD register groups</td> </tr> <tr> <td>1</td> <td>0</td> <td>FW, select D7 and D8 register groups</td> </tr> <tr> <td>1</td> <td>1</td> <td>BW, select D9 and DD register groups</td> </tr> </tbody> </table> <p>cr_ca: the data invert option for data_shift block. $dsh_shr = cr_dsh_shr \wedge cr_ca \wedge cr_mx \wedge cr_mh$ (when dsh_shr = 0, invert; when dsh_shr = 1, don't invert).</p> <table border="1"> <thead> <tr> <th>cr_dsh_shr</th> <th>cr_ca</th> <th>cr_mx=MX^ cr_36_opt[1]</th> <th>cr_mh=MH^ cr_36_opt[4]</th> <th>result</th> </tr> </thead> <tbody> <tr> <td></td> <td></td> <td></td> <td></td> <td></td> </tr> </tbody> </table>										cr_gs	cr_fv	result	0	0	FW, select D7 and D8 register groups	0	1	BW, select D9 and DD register groups	1	0	FW, select D7 and D8 register groups	1	1	BW, select D9 and DD register groups	cr_dsh_shr	cr_ca	cr_mx=MX^ cr_36_opt[1]	cr_mh=MH^ cr_36_opt[4]	result					
cr_gs	cr_fv	result																																		
0	0	FW, select D7 and D8 register groups																																		
0	1	BW, select D9 and DD register groups																																		
1	0	FW, select D7 and D8 register groups																																		
1	1	BW, select D9 and DD register groups																																		
cr_dsh_shr	cr_ca	cr_mx=MX^ cr_36_opt[1]	cr_mh=MH^ cr_36_opt[4]	result																																

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0	0	0	0	Normal
0	0	0	1	Left and right mirror
0	0	1	0	Left and right mirror
0	0	1	1	Normal
0	1	0	0	Left and right mirror
0	1	0	1	Normal
0	1	1	0	Normal
0	1	1	1	Left and right mirror
1	0	0 (default)	0 (default)	Left and right mirror
1	0	0	1	Normal
1	0	1	0	Normal
1	0	1	1	Left and right mirror
1	1	0	0	Normal
1	1	0	1	Left and right mirror
1	1	1	0	Left and right mirror
1	1	1	1	Normal

BGR : sub_pixel order of one pixel data setting ,

cr_bgr_before_en	cr_bgr_en	BGR	cr_bgr_opt	result
0	0	0	0	RGB
0	0	0	1	RGB
0	0	1	0	RGB
0	0	1	1	RGB
0	1	0	0	RGB
0	1	0	1	BGR
0	1	1	0	BGR
0	1	1	1	RGB
1	0	0	0	RGB
1	0	0	1	BGR
1	0	1	0	BGR
1	0	1	1	RGB
1	1	0	0	RGB
1	1	0	1	RGB
1	1	1	0	RGB
1	1	1	1	RGB

MX : Left and right mirror, as cr ca, see cr ca for details.

MH : Left and right mirror, as cr ca, see cr ca for details.

MY : Up and down mirror

MY	cr_36_opt[0]	result
0	0 (default)	Normal
0	1	Up and down mirror
1	0	Up and down mirror
1	1	Normal

Bit	NAME	DESCRIPTION
MY	Row Address Order	These 3bits controls MCU to memory write/read direction.
MX	Column Address Order	
MV	Row/Column Exchange	
ML	Vertical Refresh Order	LCD vertical refresh direction control '0' = LCD vertical refresh Top to Bottom '1' = LCD vertical refresh Bottom to Top
RGB	RGB-BGR ORDER	Color selector switch control '0' =RGB color filter panel, '1' =BGR color filter panel
MH	Horizontal Refresh Order	Horizontal direction '0' = Left to Right '1' = Right to Left

4.2.2.1.27 SS (37H): Scroll Start Command

8'H37	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	↑	-	cr_37_vsp[15:8]								8'h00
Par1	↑	-	cr_37_vsp[7:0]								8'h00
Description			cr_37_vsp : vertical scroll position.								

4.2.2.1.28 IDMOFF (38H): Idle Mode Off

8'H38	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Description			Without parameters, The Idle mode is displayed.								

4.2.2.1.29 IDMON (39H): Idle mode on

8'H39	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Description			Without parameters, The Idle mode is displayed, that is, the eight-color mode. Register configuration is as follows vedio mode: cr_idle_mode_en = 1 command mode: cr_idle_mode_en=1; cr_corr_col_en = 0; cr_gray_high = 'h80.								

4.2.2.1.30 COLMOD (3AH): Interface Pixel Format

8'H3A	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	↑	-	-	dpi_format[2:0]			-	dbi_format [2:0]			8'h77
Description			This command is used to define the format of RGB picture data , which is to be transferred via the MCU interface . If the customized register cr_format_cmd3a_dpi_en=1 or cr_format_cmd3a_dbi_en=1, the pixel format is configured by the 3Ah command. Otherwise, the pixel format is configured by cr_pix_format For mipi format, cr_pix_sel is set to 1								

	dpi_format[2:0]: DPI Pixel Format Definition (RGB)		
	dbi_format[2:0]: DBI Pixel Format Definition		
	The formats are shown in the table:		
	Bit	Description	
	D7	-	
	D6	RGB interface color format	
	D5		'101' = 16bit/pixel
	D4		'110' = 18bit/pixel
	D3	-	
	D2	Control interface color format	
D1	'101' = 16bit/pixel		
D0	'111' = 24 bit/pixel		
Deault: 16bits/pixel			

4.2.2.1.31 STE (44H): Set Tear Scanline

8'H44	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	↑	-						cr_44te_str[11:8]			8'h00
Par1	↑	-	cr_44te_str[7:0]								8'h00
Par2	↑	-						cr_44te_end[11:8]			8'h00
Par3	↑	-	cr_44te_end[7:0]								8'h00
Description			<p>-This command turns on the display module's Tearing Effect output signal on the TE signal line when the display module reaches line N. The TE signal is not affected by changing MV.</p> <p>-The tearing effect line on has one parameter that describes the tearing effect output line mode.</p> <p>-The tearing effect output line consist of V-blanking information only. Note that set tear scanline with N=0 is equivalent to tearing effect line on with TEM=0.</p> <p>The tearing effect output line shall be active low when the display module is in sleep mode.</p> <p>cr_44te_str: start line; cr_44te_end: indicates the end line</p> <p>When the command table2 custom register cr_te_44en =1, the TE position is configured by the 44h command, otherwise it is determined by the cr_te_str and cr_te_end of command table2.</p>								

4.2.2.1.32 GSCAN (45H): Get Scanline

8'H45	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑						cr_44te_str[11:8]			8'h00
Par1	-	↑	cr_44te_str[7:0]								8'h00
Par2	-	↑						cr_44te_end[11:8]			8'h00

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Par3	-	↑	cr_44te_end[7:0]								8'h00
Description			<p>-The display module returns the current scanline ,N, used to update the display device. The total number of scanlines on a display device is defined as VSYNC+VBP+VACT+VFP. The first scanline is defined as the first line of V Sync and is denoted as Line 0.</p> <p>-When in sleep in mode, the value returned by get scanline is undefined.</p> <p>Note: that Set Tear Scan Line with N = 0 is equivalent to Tearing Effect Line ON with M = 0.</p> <p>Read back the parameters of the 44 command</p>								

4.2.2.1.33 BL (51H): Back Light Command

8'H51	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	↑	↑	cr_bl_usr								8'h80
Description			<p>cr_bl: Adjust the backlight.</p> <p>cr_bl [7:0] is '0' when bit BCTRL of write CTRL display command (53h) is '0'</p> <p>cr_bl [7:0] is manual set brightness specified with write CTRL display command (53h) when bit BCTRL is '1' ;</p> <p>This function is to adjust the duty ratio of PWM.</p>								

4.2.2.1.34 RBL (52H): Read Display Brightness Value

8'H52	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑	cr_bl								8'h80
Description			This command returns the brightness value of the display.								

4.2.2.1.35 WRCTRLD (53H): Write CTRL Display

8'H53	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	↑	-			cr_blc trl_en		cr_dd	bl_en			8'h00
Description			<p>This command is used to control display brightness.</p> <p>cr_blcrl_en: Brightness Control Block On/Off, BCTRL=1 indicates that the brightness control function is enabled.</p> <p>cr_dd: Display Dimming On/Off. DD=1 indicates that the backlight climbing function is enabled.</p> <p>bl_en: Backlight Control On/Off, BL=1 indicates turn on the backlight. BL=0 means turn off the backlight immediately</p>								

4.2.2.1.36 RDCTRLD (54H): Read CTRL value Display

8'H54	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑			cr_blc trl_en		cr_dd	bl_en			8'h00
Description			This command returns ambient light and brightness control values. Read back the 53H command.								

4.2.2.1.37 RDFCS (AaH):Read First Checksum

8'HAa	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
-------	---	---	----	----	----	----	----	----	----	----	---------

Par0	-	↑	fst_chk_sum[15:8]								8'hff
Par1	-	↑	fst_chk_sum[7:0]								8'hff
Description			This command returns the first checksum what has been calculated from User's area registers and OTP after the write access to those registers and/or has been done.								

4.2.2.1.38 RDCFCS (AfH):Read Continue Checksum

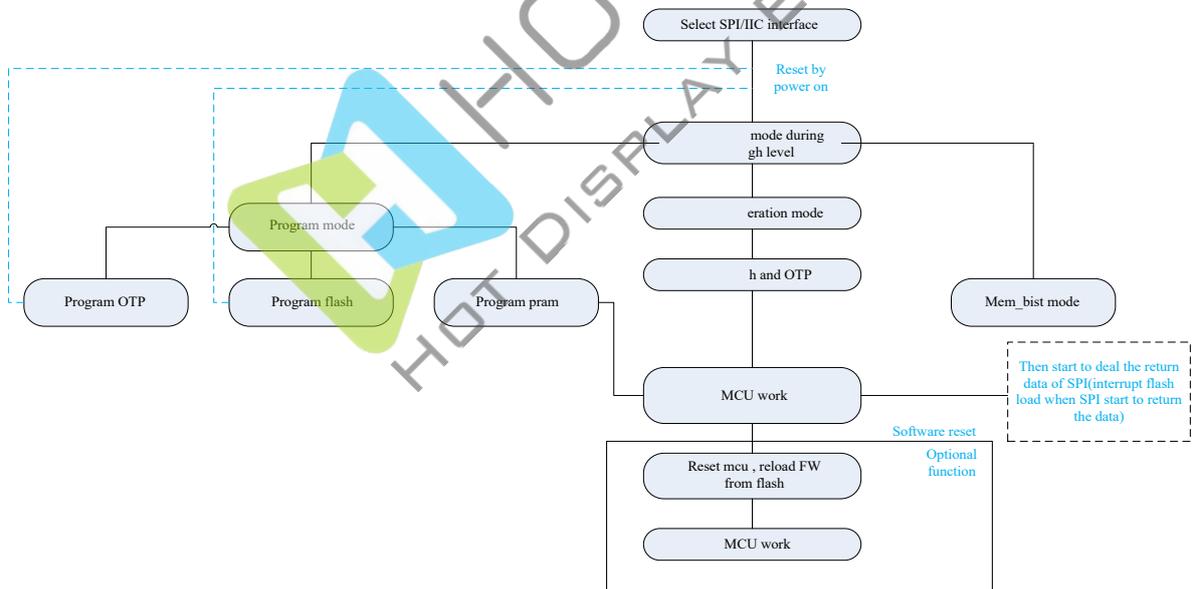
8'HAf	W	R	D7	D6	D5	D4	D3	D2	D1	D0	Default
Par0	-	↑	ctn_chk_sum[15:8]								8'hff
Par1	-	↑	ctn_chk_sum[7:0]								8'hff
Description			This command returns the continue checksum what has been calculated continuously after the first checksum has calculated from User's area registers and OTP after the write access to those registers and/or has been done.								

5 FUNCTIONS

5.1 Touch

5.1.1 TP work flow

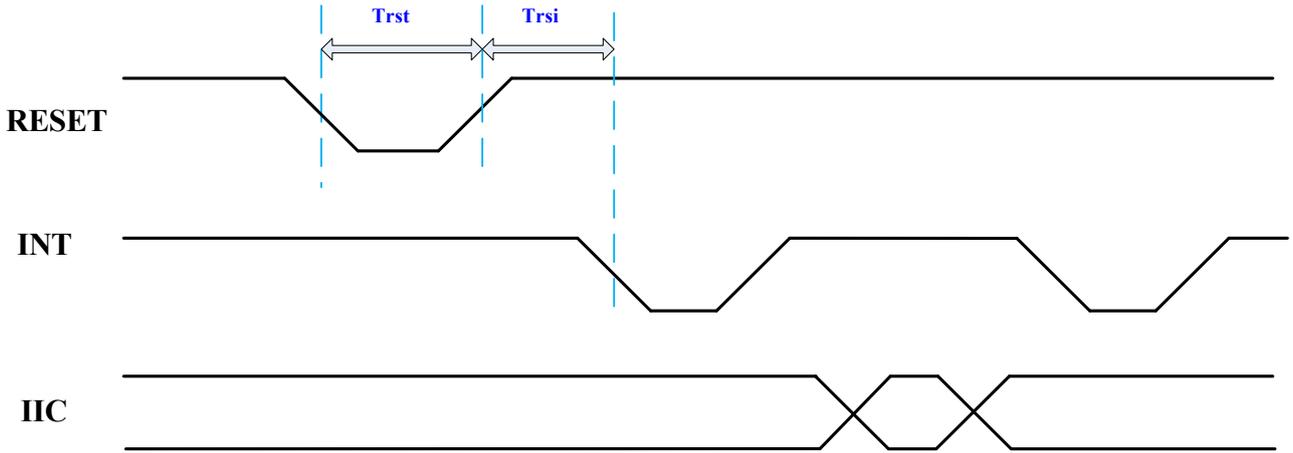
First, select the SPI or I2C interface to work through the work mode PIN. Then Write program into flash or pram with a different interface; Finally, please reset if writing program into flash or otp, and directly enter into MCU work mode if writing program into pram.



5.1.2 Touch Reset (RSTN) input timing

Reset time must be enough to guarantee reliable reset.

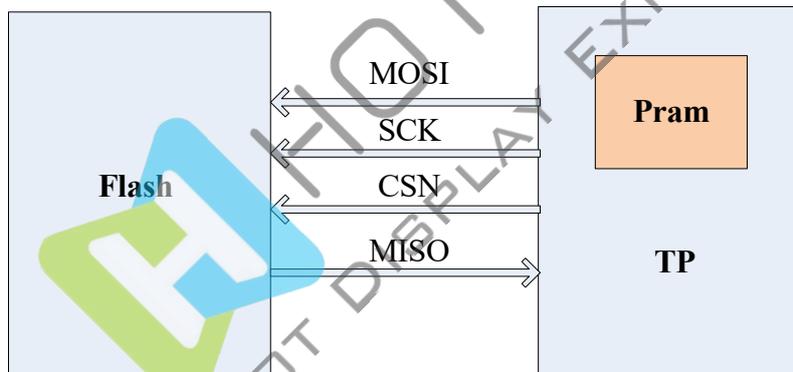
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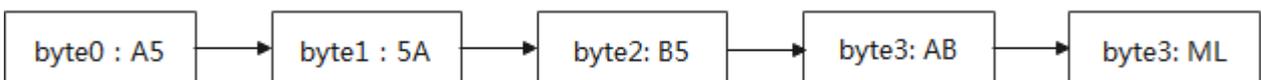
Parameter	Description	Min	Max	Units
Trsi	Time of starting to report point after resetting	200	--	ms
Trst	Reset time	5	--	ms

5.1.3 Firmware booting

Touch firmware can boot from external flash or from AP optional, default is from external flash. Boot block diagram as follows.

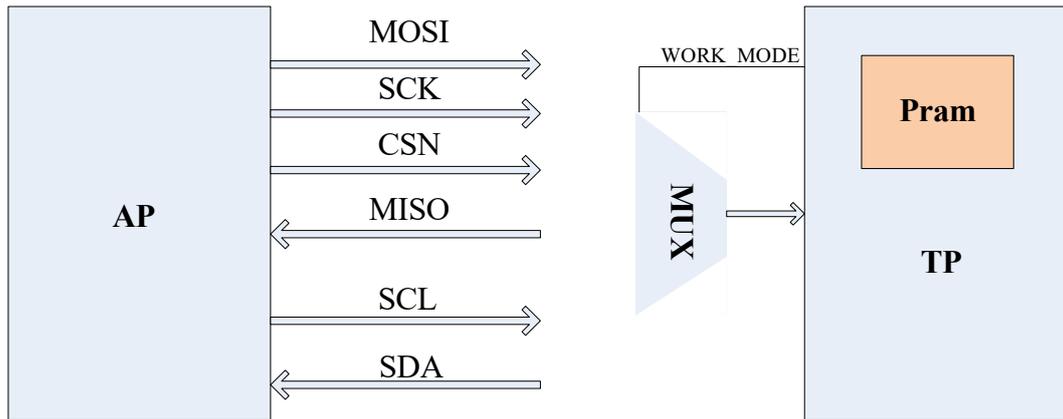


Touch controller can also boot firmware from AP through I2C or SPI interface. booting firmware protocol as follows,



byte0~byte3 is character string, it means enable booting. and ML is mode flag. when ML=1, select boot firmware from the host. it is an optional to select I2C or SPI interface through WORK_MODE pin. When WORK_MODE = 1, I2C active, otherwise, SPI active.

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5.2 Configure the color format of each interface

Color format				
Interface	cr_format_cmd3a_dpi_en=1 cr_format_cmd3a_dbi_en=X	cr_format_cmd3a_dpi_en=0 cr_format_cmd3a_dbi_en=1	cr_format_cmd3a_dpi_en=0 cr_format_cmd3a_dbi_en=0	
RGB	iformat[2:0]=dpi_format (3ah: par0 的[6:4])	format[2:0]=dbi_format (3ah: par0 的[2:0])	format[2:0]=cr_pix_format (command table2)	format[2:0]=3'b101:RGB565 format[2:0]=3'b100:RGB666 esle:RGB88
MIPI				format[2:0]=3'b111:RGB88 format[2:0]=3'b101:RGB565 format[2:0]=3'b100:RGB666 else: reserved

5.3 MIPI-DSI Interface

Connect Pin:HS_DN,HS_DP,HS_CN,HS_CP,RSTN.The MIPI Interface is selected by setting the IM[3:0] pins as “1111” level.

5.3.1 General description

The communication can be separated into two different levels between the host and the display module:

- Interface Level: Low level communication, low power
- Packet level: High level communication, high speed

5.3.2 Interface level communication

5.3.2.1 General

The display module uses data and clock lane differential pairs for DSI. Both clock lane and data lane can be driven in Low Power (LP) or High Speed (HS) mode.

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-	Lane support mode	MPU(Host) AXS15260D-S1(Slave)
Clock Lane	Unidirectional lane •High-Speed Clock only •SimplifiedEscape Mode (ULPS Only)	
Data Lane	Bi-directional lane • Forward high-speed only •Bi-directional Escape Mode •Bi-direction LPDT	

Table: Lane types and support mode

Low Power mode means that each line of the differential pair is used in single end mode and a differential receiver is disabled (The termination resistor of the receiver is disabled) and it can be driven into a low power mode.

High Speed mode means that differential pairs (The termination resistor of the receiver is enabled) are not used in the single end mode.

There are different modes and protocols in each mode when transferring information from the HOST to the display module and vice versa.

The State Codes of the High Speed (HS) and Low Power (LP) lane pair are defined below.

Lane Pair State Code	Line DC Voltage Levels		High Speed (HS)	Low-Power (LP)	
	Dn+ Line	Dn- Line	Burst Mode	Control Mode	Escape Mode
HS-0	Low (HS)	High (HS)	Differential-0	Note 1	Note 1
HS-1	High (HS)	Low (HS)	Differential-1	Note 1	Note 1
LP-00	Low (LP)	Low (LP)	Not Defined	Bridge	Space
LP-01	Low (LP)	High (LP)	Not Defined	HS-Request	Mark-0
LP-10	High (LP)	Low (LP)	Not Defined	LP-Request	Mark-1
LP-11	High (LP)	High (LP)	Not Defined	Stop	Note 2

Table: High Speed and Low-Power Lane Pair State Descriptions

5.3.2.2 DSI-CLK lanes

DSI-CLK+/- lanes can be driven into three different power modes: Low Power Mode (LPM LP-11), Ultra Low Power Mode (ULPM) or High Speed Clock Mode (HSCM).

Clock lanes are in a single end mode (LP = Low Power) when there is entering or leaving Low Power Mode(LPM) or Ultra Low Power Mode (ULPM).

Clock lanes are in the single end mode (LP = Low Power) when there is entering in or leaving

out High Speed Clock Mode (HSCM).

These entering and leaving protocols are using clock lanes in the single end mode to generate an entering or leaving sequences.

The principal flow chart of the different clock lanes power modes is illustrated below.

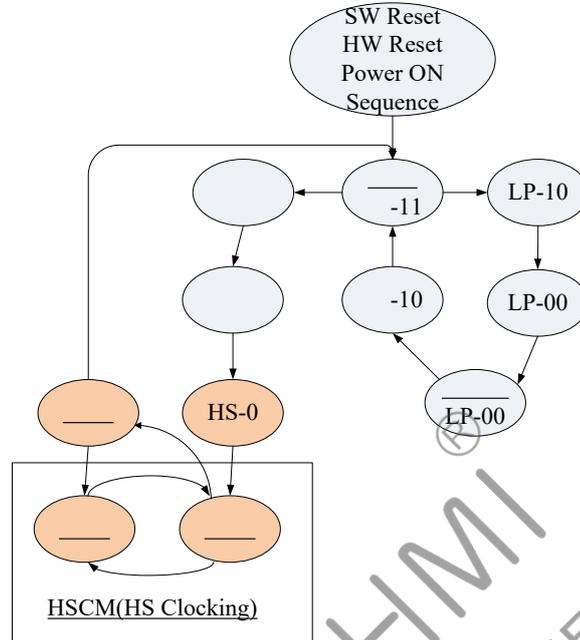


Figure: Clock Lanes Power Modes

Notes:

1. Low-Power Receivers (LP-Rx) of the lane pair are checking the LP-00 state code, when the Lane Pair is in the High Speed (HS) mode.

2. If Low-Power Receivers (LP-Rx) of the lane pair recognizes LP-11 state code, the lane pair returns to LP-11 of the Control Mode.

Low Power Mode (LPM)

DSI-CLK+/- lanes can be driven to the Low Power Mode (LPM), when DSI-CLK lanes are entering the LP-11 State Code, in three different ways:

1) After SW Reset, HW Reset or Power On Sequence =>LP-11

2) After DSI-CLK+/- lanes are leaving Ultra Low Power Mode (ULPM, LP-00 State Code) =>LP-10 =>LP-11 (LPM). This sequence is illustrated below.

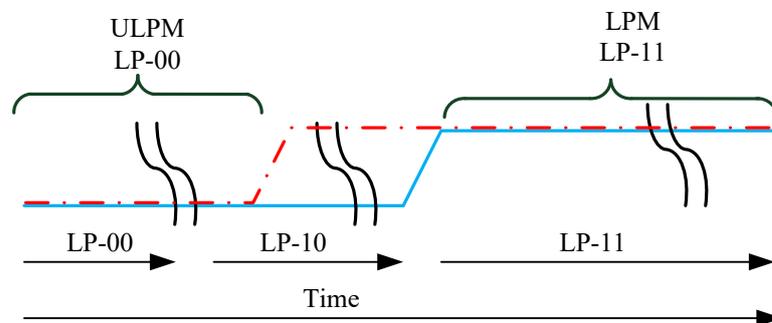


Figure:From ULPM to LPM

After DSI-CLK+/- lanes are leaving High Speed Clock Mode (HSCM, HS-0 or HS-1 State

Code) =>HS-0 =>LP-11 (LPM). This sequence is illustrated below.

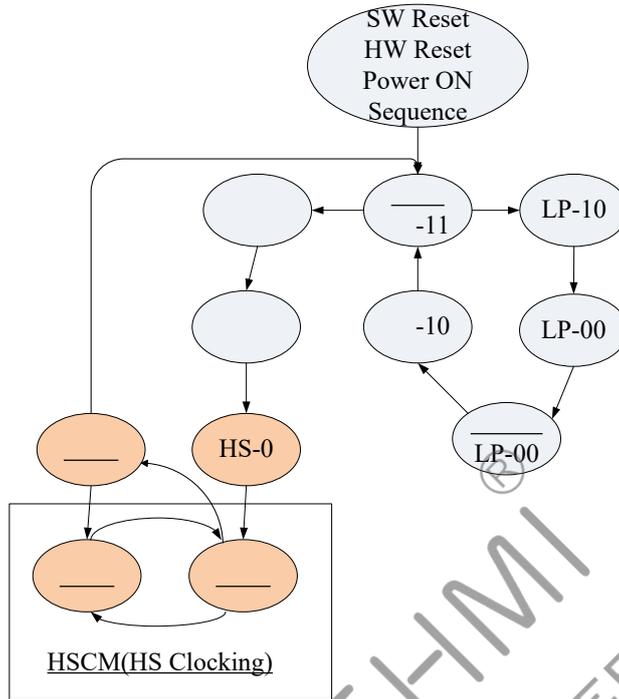


Figure: From HSCM to LPM

All three mode changes are illustrated a flow chart below.

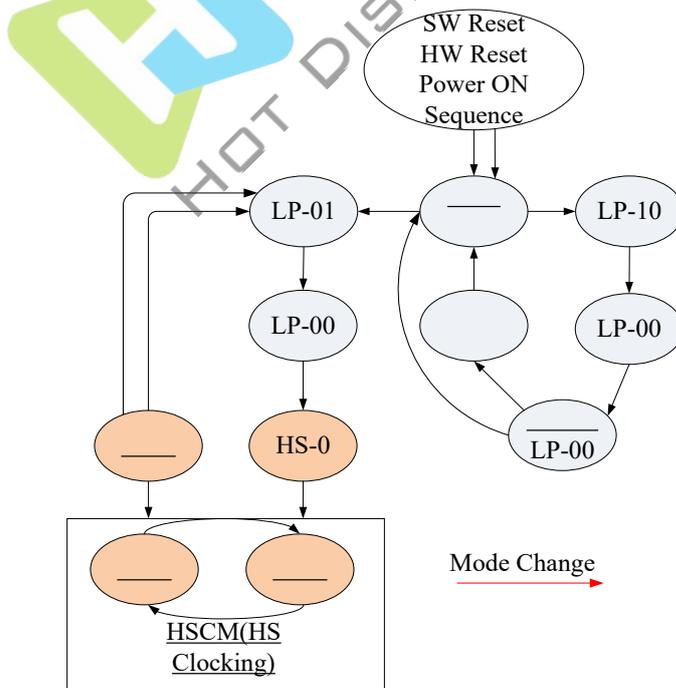


Figure: All three mode changes to LPM

Ultra Low Power Mode (ULPM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

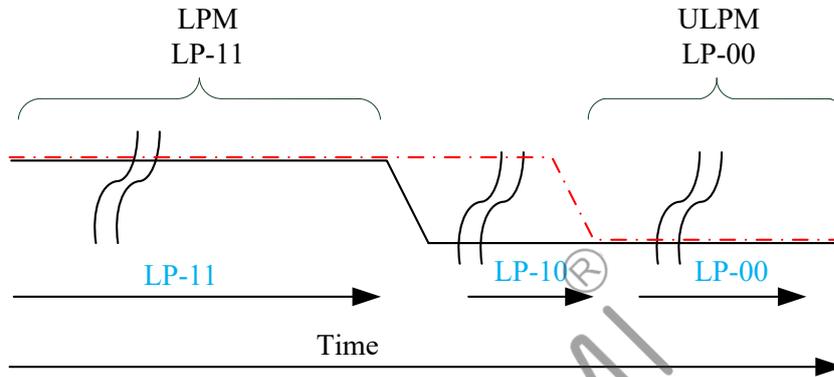


Figure: From LPM to UPLM

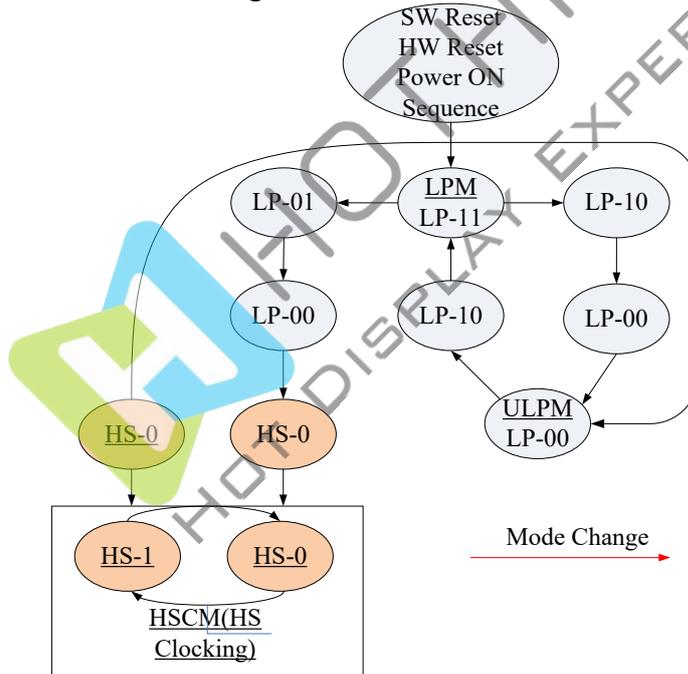


Figure: The mode change from LPM to UPLM

High-speed Clock Mode (HSCM)

DSI-CLK+/- lanes can be driven to the High Speed Clock Mode (HSCM), when DSI-CLK lanes are starting to work between HS-0 and HS-1 State Codes.

The only entering possibility is from the Low Power Mode (LPM, LP-11 State Code) =>LP-01 =>LP-00 =>HS-0 =>HS-0/1 (HSCM). This sequence is illustrated below.

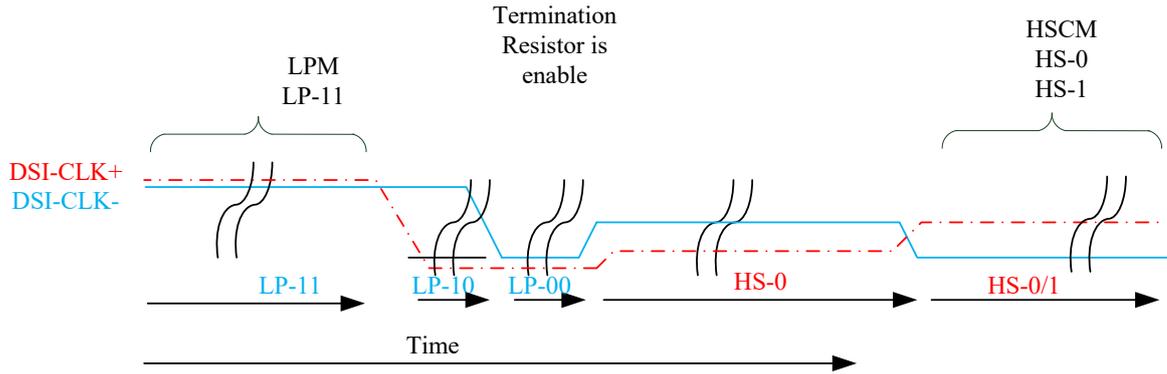


Figure: From LPM to HSCM

The mode change is also illustrated below:

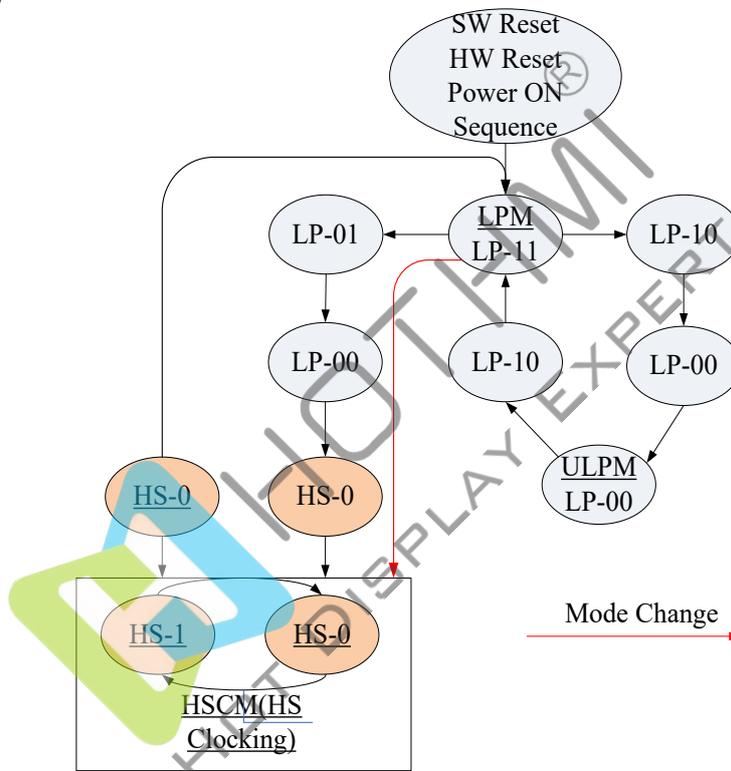


Figure: Mode change from LPM to HSCM

The high speed clock (DSI-CLK+/-) is started before high speed data is sent via DSI-Dn+/- lanes. The high speed clock continues clocking after the high speed data sending has been stopped

The burst of the high speed clock consists of:

- Even the number of transitions
- Start state is HS-0
- End state is HS-0

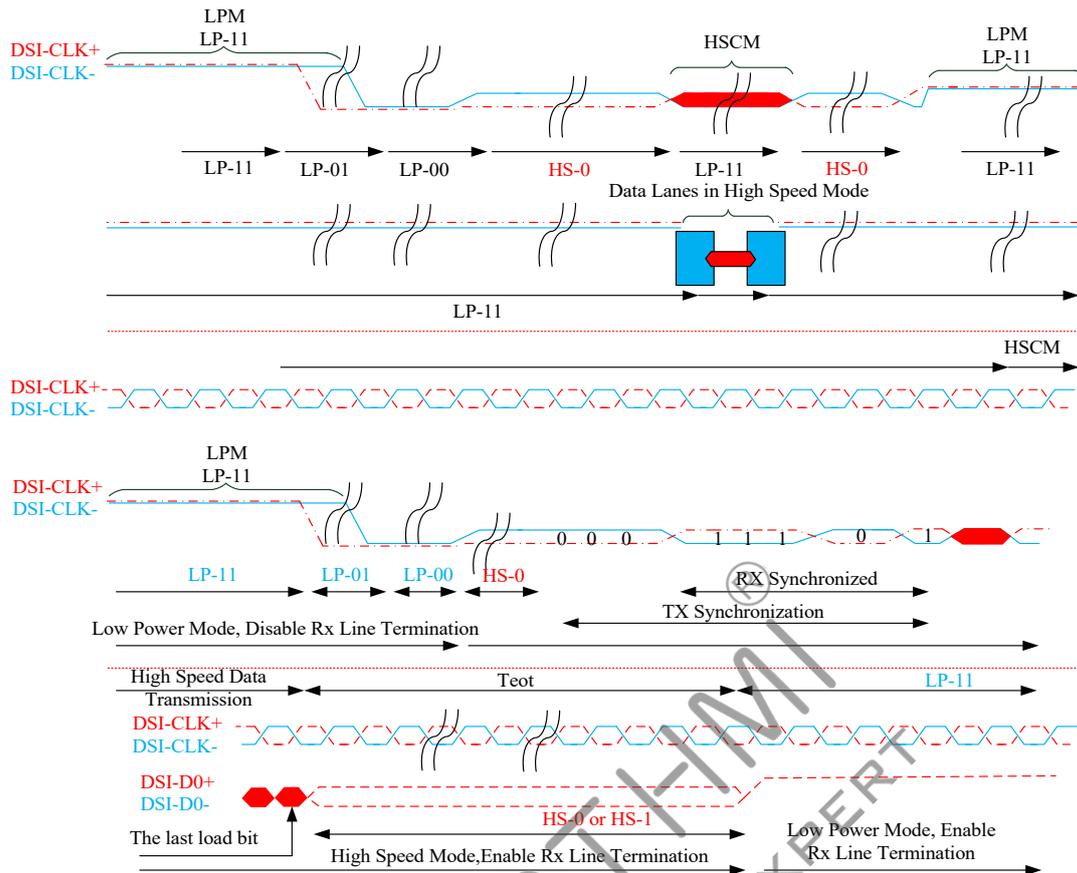


Figure: High speed clock burst

5.3.3 DSI data lanes

5.3.3.1 General

DSI-Dn+/- Data Lanes can be driven in different modes which are:

- Escape Mode (only support DSI_D0 data lane pair)
- High-Speed Data Transmission (support all data lane pairs)
- Bus Turnaround Request (only support DSI_D0 data lane pair)

These modes and their entering codes are defined in the following table.

Mode	Entering Mode Sequence	Leaving Mode Sequence
Escape Mode	LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00	L P-00 =>LP-10 =>LP-11 (Mark-1)
High-Speed Data Transmission	LP-11 =>LP-01 =>LP-00 =>HS-0	(HS-0 or HS-1) =>LP-11
Bus Turnaround Request	LP-11 =>LP-10 =>LP-00 =>LP-10 =>LP-00	High-Z, Note

Table: Entering and leaving sequences

5.3.3.2 Escape modes

Escape mode is a special mode of operation for Data Lanes using Low-Power states. With this mode, some additional functionality becomes available. Escape mode operation shall be supported in the Forward direction and Reverse direction.

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The basic sequence of the Escape Mode is as follows

- Start: LP-11.
- Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00.
- Escape Command, which is coded, when one of the data lanes is changing from low-to-high-to-low, then this changed data lane is presenting a value of the current data bit.
 - A payload stream if it is needed.
- Exit Escape (Mark-1) LP-00 =>LP-10 =>LP-11.
- End: LP-11.

For Data Lane0, once Escape mode is entered, the transmitter shall send an 8-bit entry command to indicate the requested action. All currently available Escape mode commands and actions are listed below.

- Send or receive “Low-Power Data Transmission” (LPDT).
- Driver data lanes to “Ultra-Low Power State” (ULPS).
- Indicate “Remote Application Reset” (RAR), which is resetting the display module (same as S/W Reset function).
- Indicate “Tearing Effect” (TEE), which is used for a TE line event from the display module to the HOST.
- Indicate “Acknowledge” (ACK), which is used for a non-error event from the display module to the HOST.

The Stop state shall be used to exit Escape mode and cannot occur during Escape mode operation because of the Spaced-One-Hot encoding. Stop state immediately returns the Lane to Control mode. If the entry command doesn't match a supported command, that particular Escape mode action shall be ignored and the receive side waits until the transmit side returns to the Stop state. For Data Lane1 and 2, only support ULPS Escape mode commands.

- Driver data lanes to “Ultra-Low Power State” (ULPS).

The basic construction is illustrated below:

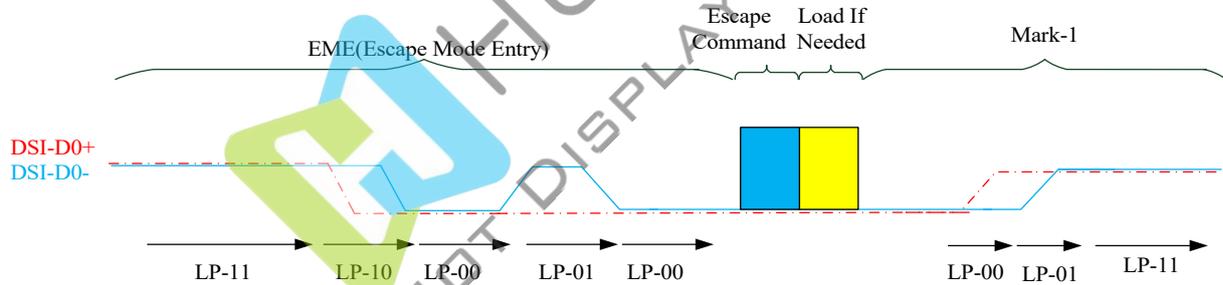


Figure: General Escape mode sequence

The number of the different Escape Commands is eight. These eight different Escape Commands can be divided to 2 different groups: Mode or Trigger. Escape command and groups are defined below.

Escape Command	Command Type Mode/Trigger	Entry Command Pattern (First Bit => Last Bit Transmitted)
Low-Power Data Transmission	Mode	1110 0001bin
Ultra-Low Power Mode	Mode	0001 1110bin
Remote Application Reset	Trigger	0110 0010 bin
Tearing Effect	Trigger	0101 1101 bin

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Acknowledge	Trigger	0010 0001 bin
-------------	---------	---------------

Table: Escape commands

The HOST is inform the display module that it is controlling data lanes (DSI-D0+/-) with the Mode e.g. The HOST can inform the display module that it can put data lanes in the low power mode.

The HOST is waiting from the display module event information, which has been set by the HOST , with the Trigger e.g. when the display module reaches a new V-synch, the display module sent the HOST a TE trigger (TEE), if the HOST has been requested it.

Low-Power Data Transmission (LPDT)

The HOST can send data to the display module in Low-Power Data Transmission (LPDT) mode when data lanes are entering in Escape Mode and Low-Power Data Transmission (LPDT) command has been sent to the display module. The display module is also using the same sequence when it is sending data to the HOST .

The Low Power Data Transmission (LPDT) is using a following sequence:

- Start: LP-11
 - Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
 - Low-Power Data Transmission (LPDT) command in Escape Mode: 1110 0001 (First to Last bit)
 - Payload (Data):
 - One or more bytes
 - Data lanes are in pause mode when data lanes are stopped (Both lanes are low) between bytes
 - Mark-1: LP-00 =>LP-10 =>LP-11
 - End: LP-11
- This sequence is illustrated for reference purposes below:

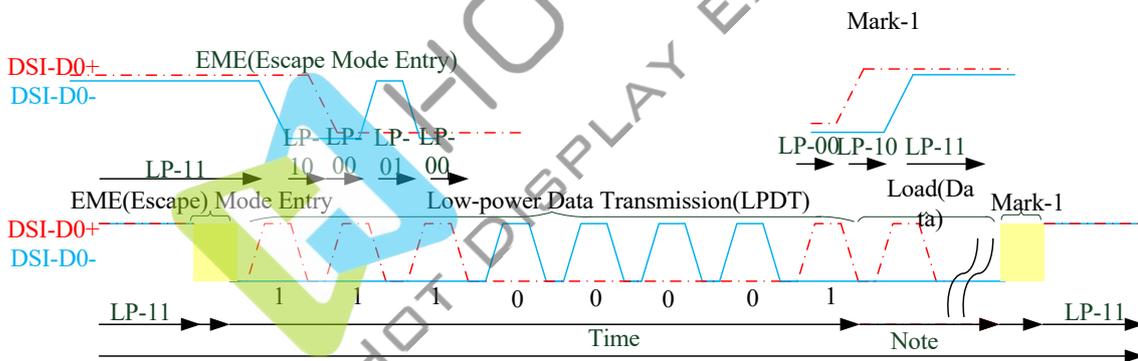


Figure: Low-power data transmission

Note: Load(Data) is presenting the first bit is logical “1” in this example

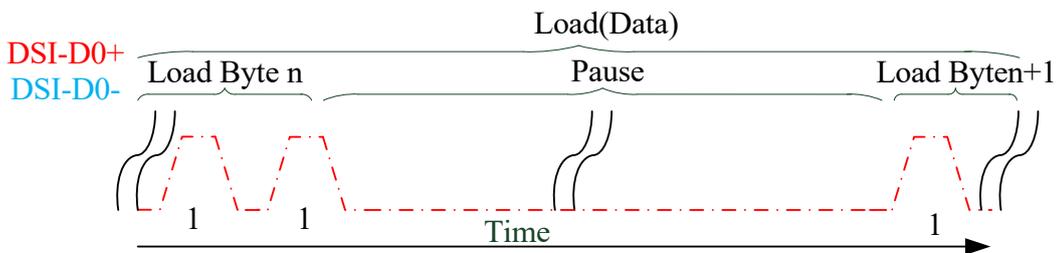


Figure: Pause (example)

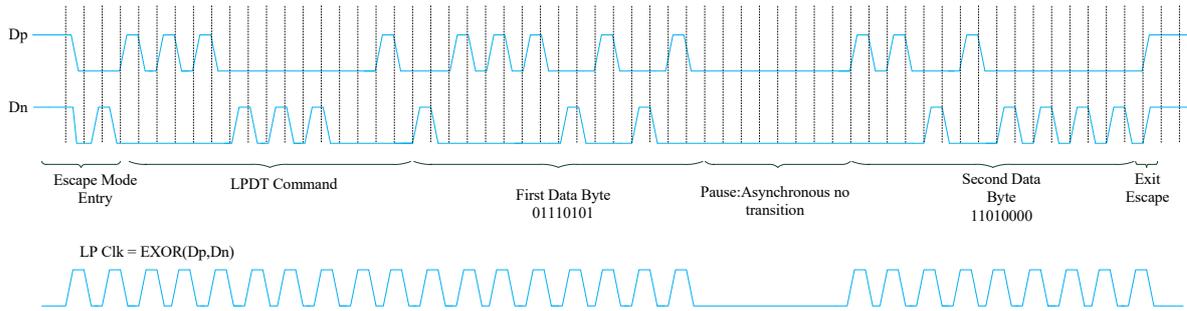


Figure: Two Data Byte Low-Power Data Transmission Example

Ultra-Low Power State (ULPS)

The HOST can force data lanes in Ultra-Low Power State (ULPS) mode when data lanes are entering in Escape Mode.

The Ultra-Low Power State (ULPS) used/uses(?) the following sequence:

- Start: LP-11
- Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Ultra-Low Power State (ULPS) command in Escape Mode: 0001 1110 (First to Last bit)
- Ultra-Low Power State (ULPS) when the HOST is keeping data lanes low
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

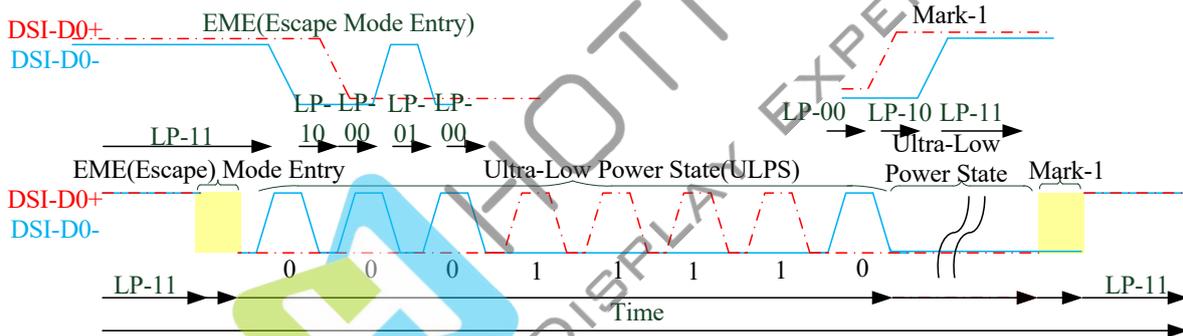


Figure: Ultra-low power state (ULPS)

Remote Application Reset (RAR)

The HOST can inform the display module that it should be reseted in Remote Application Reset (RAR) trigger when data lanes are entering in Escape Mode. The Remote Application Reset using the following sequence:

- Start: LP-11
- Escape Mode Entry : LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Remote Application Reset (RAR) command in Escape Mode: 0110 0010 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

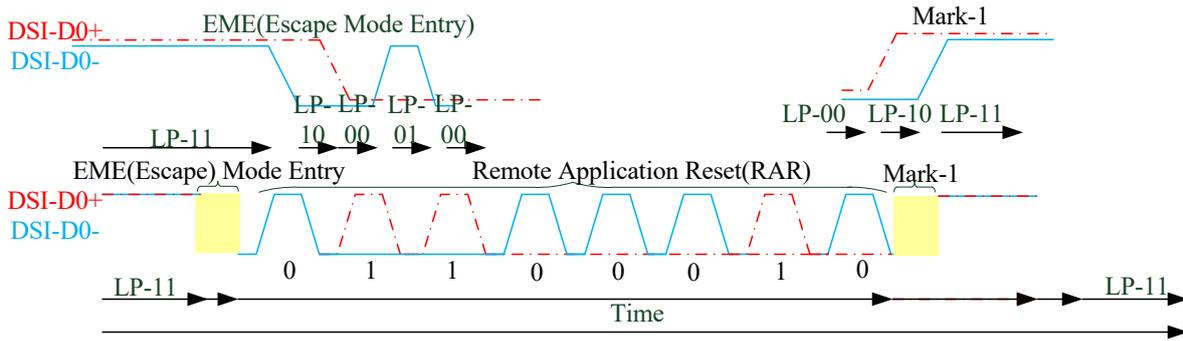


Figure: Remote Application Reset (RAR)

Tearing Effect (TEE)

The display module can inform the HOST when a tearing effect event (New V-synch) has been happen on the display module by Tearing Effect (TEE).

The Tearing Effect (TEE) is using a following sequence:

- Start: LP-11
- Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Tearing Effect (TEE) trigger in Escape Mode: 0101 1101 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

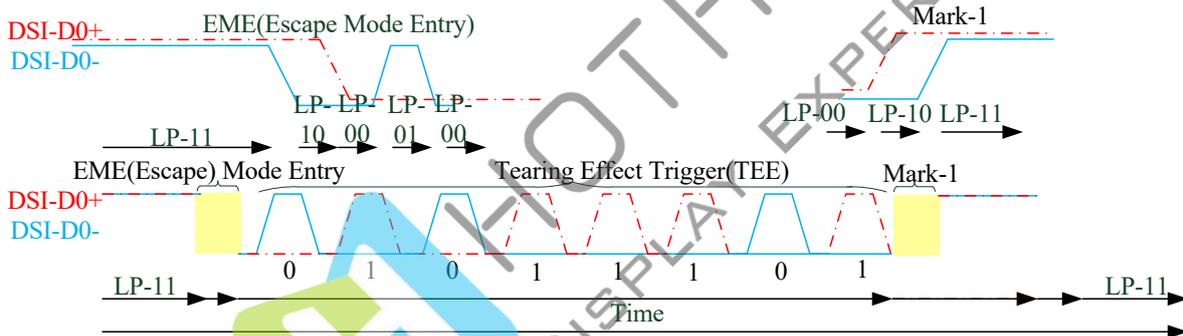


Figure: Tearing effect(TEE)

Acknowledgement (ACK)

The display module can inform the HOST when an error has not recognized on it by Acknowledge (ACK).

The Acknowledge (ACK) used/uses(?) the following sequence:

- Start: LP-11
- Escape Mode Entry: LP-11 =>LP-10 =>LP-00 =>LP-01 =>LP-00
- Acknowledge (ACK) command in Escape Mode: 0010 0001 (First to Last bit)
- Mark-1: LP-00 =>LP-10 =>LP-11
- End: LP-11

This sequence is illustrated for reference purposes below:

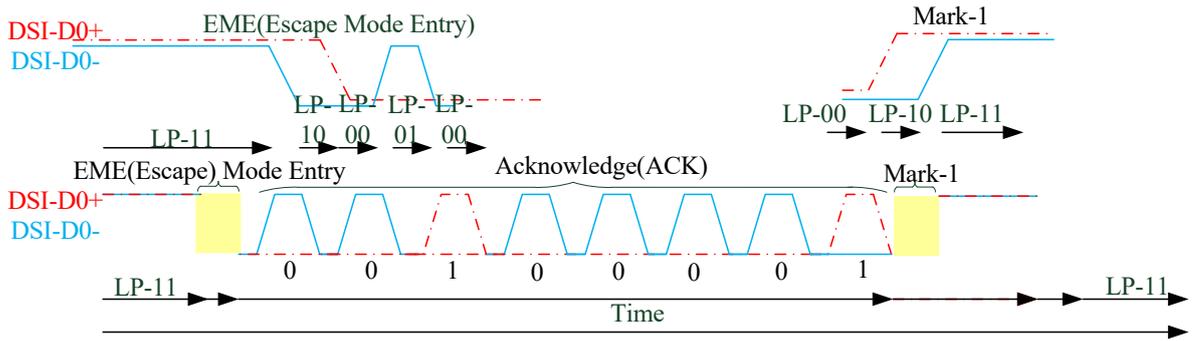


Figure: Acknowledgement (ACK)

5.3.3.3 High-Speed Data Transmission (HSDT)

Entering High-Speed Data Transmission (T_{sot} of HSDT)

The display module is entering High-Speed Data Transmission (HSDT) when Clock lanes DSI-CLK+/- have already been entered in the HighSpeed Clock Mode (HSCM) by the HOST. See more information on chapter “High-Speed Clock Mode (HSCM)”.

Data lanes DSI-D0+/- of the display module are entering (T_{SOT}) in the High-Speed Data Transmission(HSDT) as follow

- Start: LP-11
- HS-Request: LP-01
- HS-Settle: LP-00 => HS-0 (Rx: Lane Termination Enable)
- Rx Synchronization: 011101 (Tx (= HOST) Synchronization: 0001 1101)
- End: High-Speed Data Transmission (HSDT) – Ready to receive High-Speed Data Load

This same entering High-Speed Data Transmission (T_{SOT} of HSDT) sequence is illustrated below.

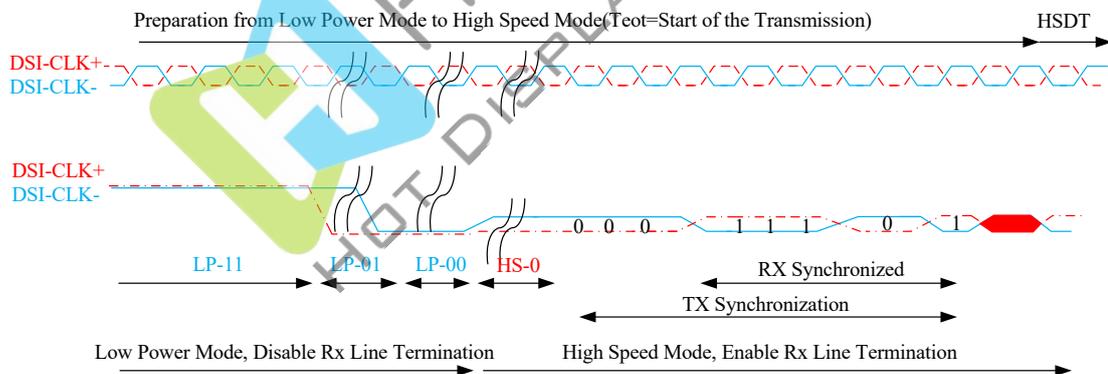


Figure: T_{sot} of HSDT

Leaving High-Speed Data Transmission (T_{EOt} of HSDT)

The display module is leaving the High-Speed Data Transmission (T_{EOt} of HSDT) when Clock lanes DSI-CLK+/- are in the High-Speed Clock Mode (HSCM) by the HOST and this HSCM is kept until data lanes DSI-D0+/- are in LP-11 mode. See more information on chapter “7.2.2 High-Speed Clock Mode (HSCM)”. Data lanes DSI-D0+/- of the display module are leaving from the High-Speed Data Transmission (T_{EOt} of HSDT) as follow

- Start: High-Speed Data Transmission (HSDT)
- Stops High-Speed Data Transmission
- HOST changes to HS-1, if the last load bit is HS-0
- HOST changes to HS-0, if the last load bit is HS-1

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- End: LP-11 (Rx: Lane Termination Disable)

The same leaving High-Speed Data Transmission (TEOT of HSDT) sequence is illustrated below

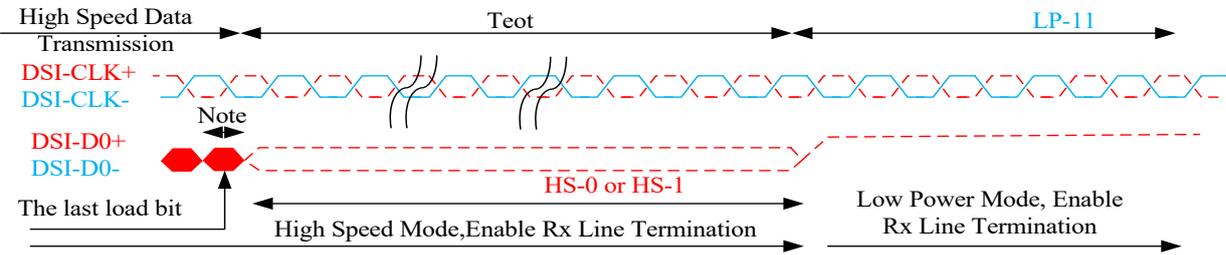


Figure: TEOT of HSDT

Note:

If the last load bit is HS0, the transmitter changes from HS0 to HS-1.

If the last load bit is HS1, the transmitter changes from HS1 to HS-0.

Burst of the High-Speed Data Transmission (HSDT)

The burst of the high-speed data transmission (HSDT) can consist of one data packet or several data packets. These data packets can be Long (LPa) or Short (SPa) packets. These packets are defined on chapter “Short Packet (SPa) and Long Packet (LPa) Structures“. These different burst of the High-Speed Data Transmission (HSDT) cases are illustrated for reference purposes below.

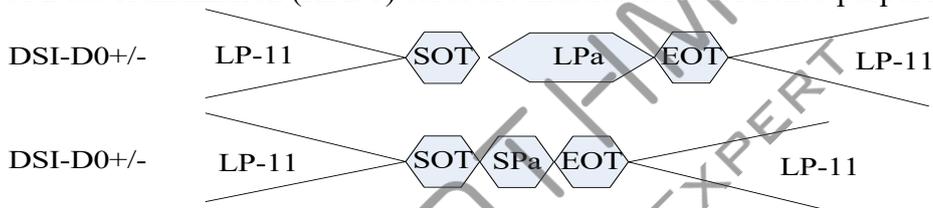


Figure: Single packet in HSDT

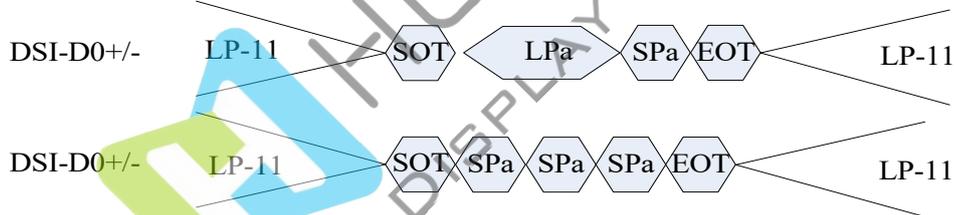


Figure: Multiple packets in HSDT

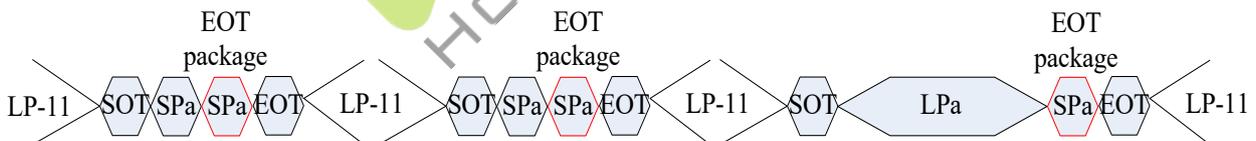


Figure: Packets with EoT package in HSDT

Abbreviation	Explanation
LP-11	Low Power Mode, Data lanes are '1's (Stop Mode)
SOT	Start of the Transmission
LPa	Long Packet
SPa	Short Packet
EOT	End of the Transmission

Table: Abbreviations

5.3.3.4 Bus Turnaround (BTA)

The HOST or display module, which is controlling DSI-D0+/- Data Lanes, can start a bus turnaround procedure when it wants information to a receiver.

The HOST and display module can use the same sequence when this bus turnaround procedure is used.

This sequence is described for reference purposes, when the HOST wants to do the bus turnaround procedure to the display module, as follows.

- Start (HOST): LP-11
- Turnaround Request (HOST): LP-11 =>LP-10 =>LP-00
- The HOST waits until the display module is starting to control DSI-D0+/- data lanes and the HOST stops to control DSI-D0+/- data lanes (= High-Z)
- The display module changes to the stop mode: LP-00 =>LP-10 =>LP-11

The same bus turnaround procedure (From the HOST to the display module) is illustrated below.

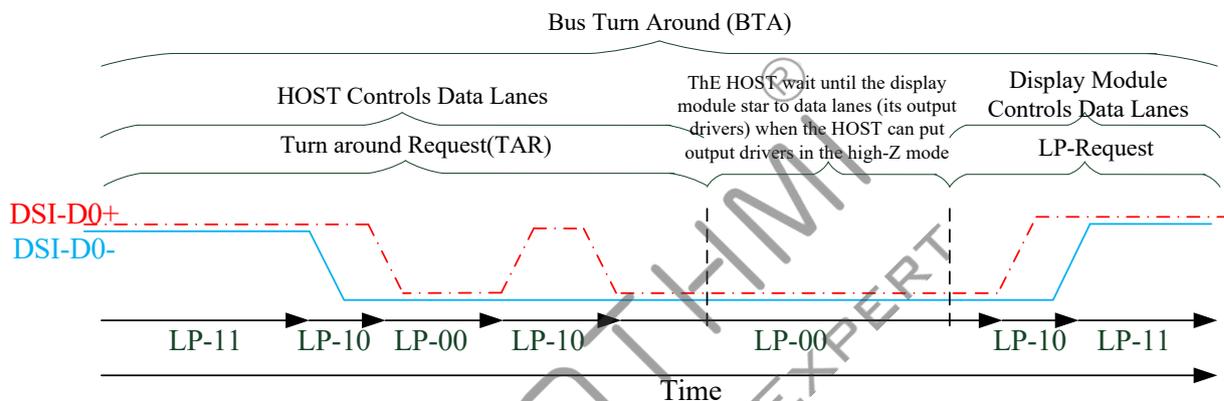


Figure: Bus turnaround procedure

5.3.4 Packet level communication

5.3.4.1 Short Packet (SPa) and Long Packet (LPa) structures

Short Packet (SPa) and Long Packet (LPa) are always used when data transmission is done in Low Power Data Transmission (LPDT) or High-Speed Data Transmission (HSMT) modes.

The lengths of the packets are

- Short Packet (SPa): 4 bytes
- Long Packet (LPa): From 6 to 65,541 bytes

The type (SPa or LPa) of the packet can be recognized from their package headers (PH).

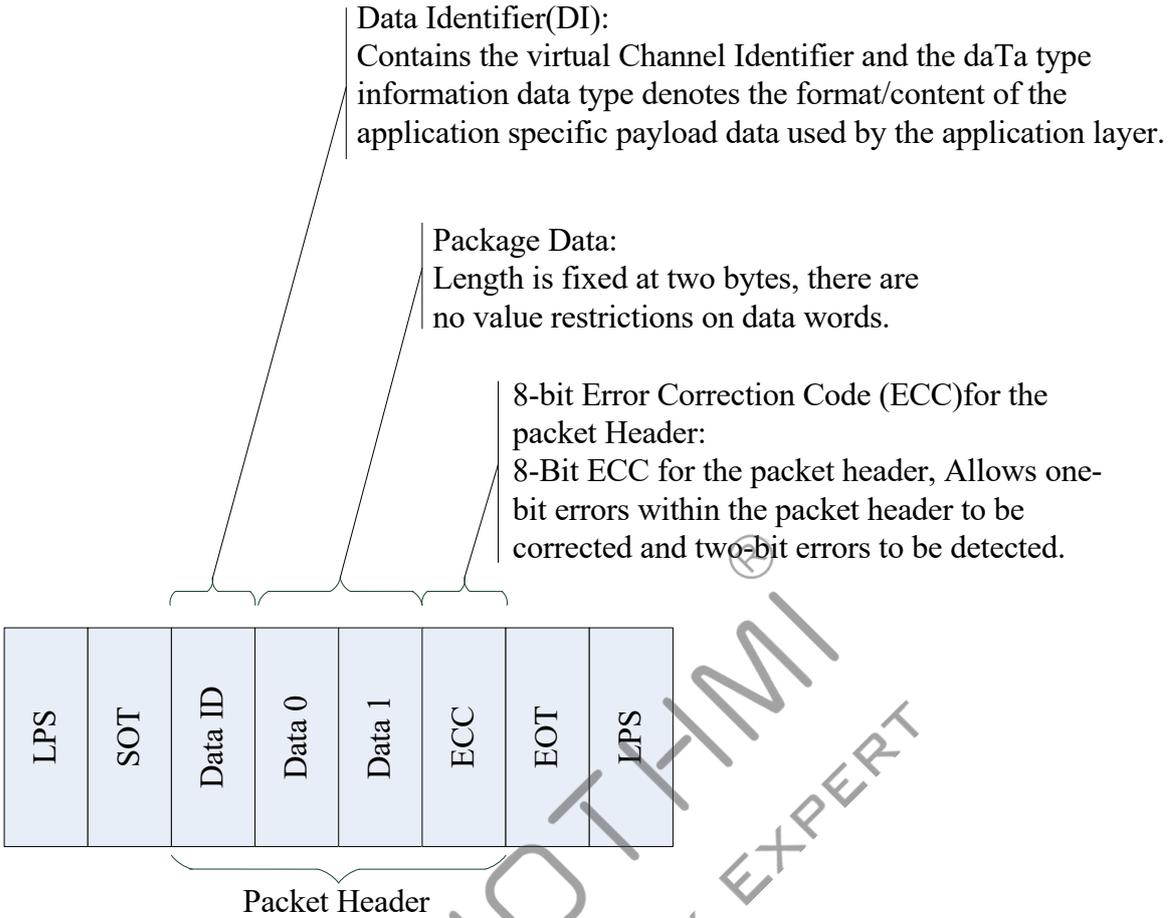
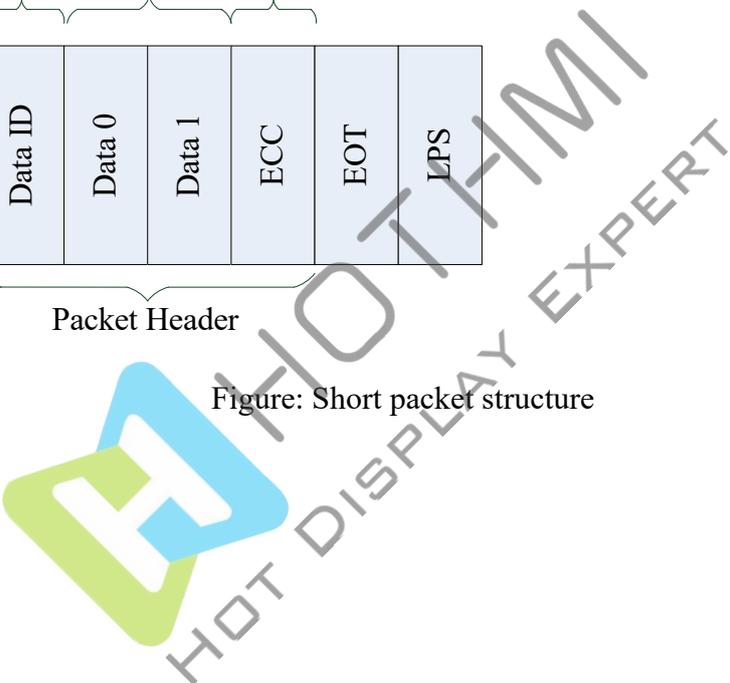


Figure: Short packet structure



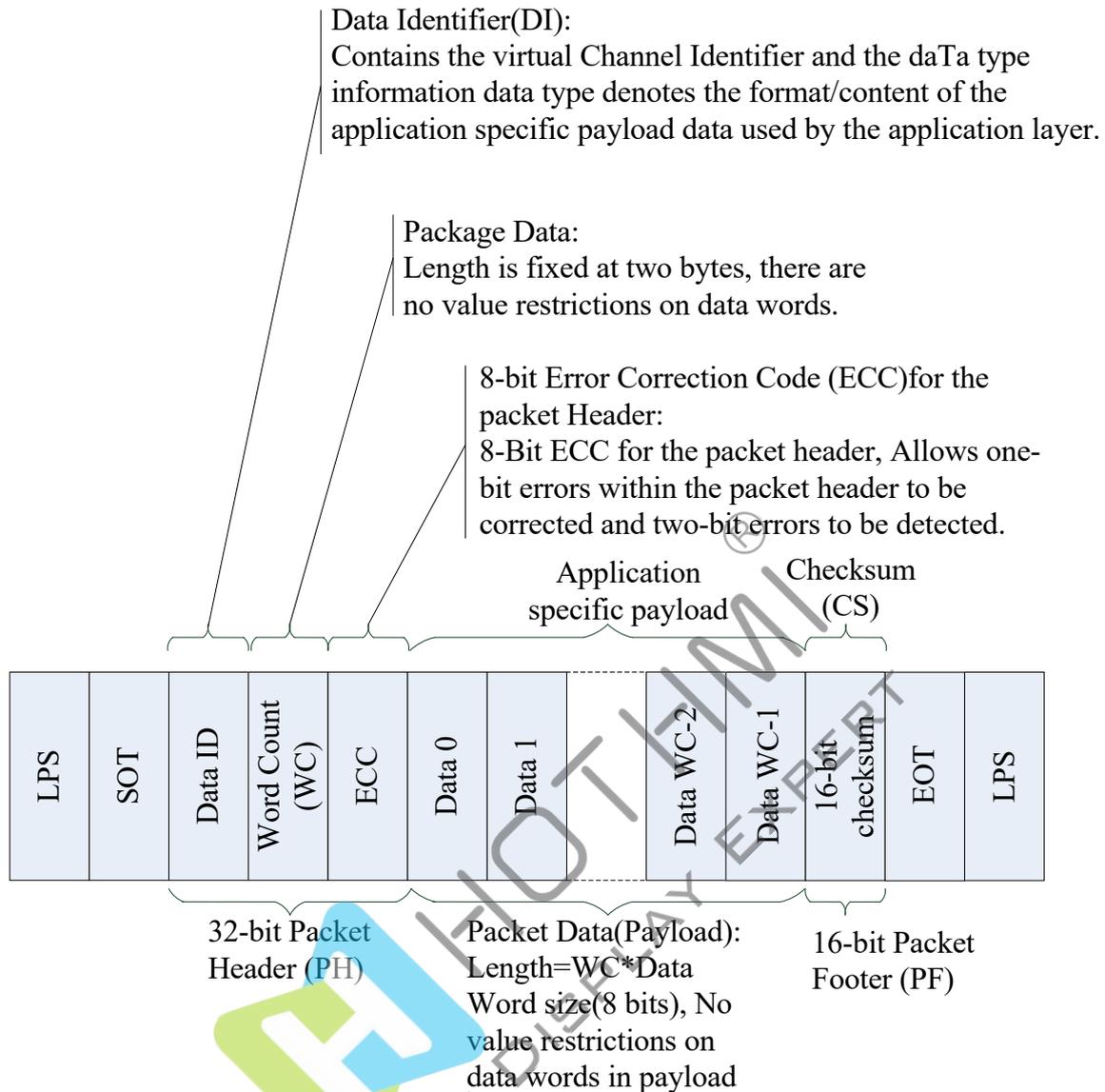


Figure.: Long packet structure

Note: Short Packet (SPa) Structure” and Long Packet (LPa) Structure” are presenting a single packet sending (= Includes LP-11, SoT and EoT for each packet sending).

The other possibility is that there is not needed SoT, EoT and LP-11 between packets if packets have sent in multiple packet format. e.g.:

- LP-11 =>SoT =>SPa =>LPa =>SPa =>SPa =>EoT =>LP-11
- LP-11 =>SoT =>SPa =>SPa =>SPa =>EoT =>LP-11
- LP-11 =>SoT =>LPa =>LPa =>LPa =>EoT =>LP-11

Bit Order of the Byte on Packets

A byte is the smallest transmission unit of a packet. Sequentially, a transmitter shall send data LSB first, MSB last. For packets with multi-byte fields, the least significant byte shall be transmitted first unless otherwise specified. Figure below shows a complete Long packet data transmission. Note, the figure shows the byte values in standard positional notation, i.e. MSB on the left and LSB on the right, while the bits are shown in chronological order with the LSB on the left, the MSB on the right and time increasing left to right.

DI	WC(Least Significant Byte)	ECC	Data	CRC(LS Byte)	CRC(MS Byte)
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39hex				01hex				15hex				01hex				0Ehex				1Ehex																											
1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1	1	0	0	0	0	0	0
L				N	L			N	L			N	L			N	L			N	L			N	L			N	L			N	L			N	L			N	L			N	L		
S				S	S			S	S			S	S			S	S			S	S			S	S			S	S			S	S			S	S			S	S			S	S		
B				B	B			B	B			B	B			B	B			B	B			B	B			B	B			B	B			B	B			B	B			B	B		

Figure: Bit order of the byte on packets

Byte Order of the Multiple Byte Information on Packets

Byte order of the multiple bytes information, what is used on packets, is that the Least Significant (LS) Byte of the information is sent in the first and the Most Significant (MS) Byte of the information is sent in the last. e.g. Word Count (WC) consists of 2 bytes (16 bits) when the LS byte is sent in the first and the MS byte is sent in the last.

This same order is illustrated for reference purposes below.

WC(Least Significant Byte)								WC(Most Significant Byte)							
01hex								00hex							
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
B0	B1	B2	B3	B4	B5	B6	B7	B8	B9	B10	B11	B12	B13	B14	B15
L							M	L							M
S							S	S							S
B							B	B							B

Figure: Byte order of the multiple byte information on packets

Packet Head (PH)

The packet header is always consisting of 4 bytes. The content of these 4 bytes are different when it is used to Short Packet (SPa) or Long Packet (LPa).

Short Packet (SPa):

- 1st byte: Data Identification (DI) => Identification that this is Short Packet (SPa)
- 2nd and 3rd bytes: Packet Data (PD), Data 0 and 1
- 4th byte: Error Correction Code (ECC)

DI				Data 0				Data 1				ECC											
15hex				3Ahex				07hex				18hex											
1	0	1	0	1	0	0	0	0	1	0	1	1	1	0	0	0	0	0	1	1	0	0	0
B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5
L				M	L			M	L			M	L			M	L			M	L		
S				S	S			S	S			S	S			S	S			S	S		
B				B	B			B	B			B	B			B	B			B	B		

Figure: Packet head on short packet

Long Packet (LPa):

- 1st byte: Data Identification (DI) => Identification that this is Long Packet (LPa)
- 2nd and 3rd bytes: Word Count (WC)
- 4th byte: Error Correction Code (ECC)

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DI								WC(Least Significant Byte)								WC(Most Significant Byte)								ECC														
39hex								01hex								00hex								15hex														
1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0					
B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B
L								M	L						M	L							M	L							M	L						
S								S	S						S	S							S	S							S	S						
B								B	B						B	B							B	B							B	B						

Figure: Packet head on long packet

Data Identification

Data Identification (DI) is a part of Packet Header (PH) and it consists of 2 parts:

- Virtual Channel (VC), 2 bits, DI[7...6]
- Data Type (DT), 6 bits, DI[5...0]

The Data Identification (DI) structure is illustrated on a table below.

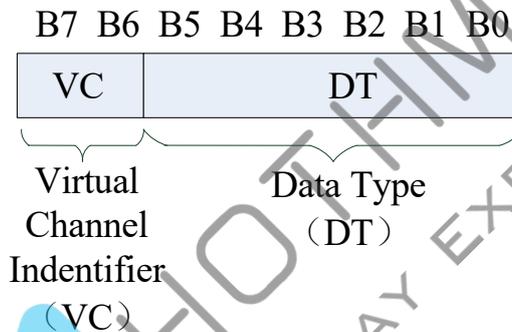


Table: Data identification structure

Data Identification (DI) is illustrated on Packet Header (PH) for reference purposes below.

DI								WC(Least Significant Byte)								WC(Most Significant Byte)								ECC							
39hex								01hex								00hex								15hex							
1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	
L								M	L						M	L							M	L							
S								S	S						S	S							S	S							
B								B	B						B	B							B	B							

Figure: Data identification of the packet head

Virtual Channel (VC)

A processor may service up to four peripherals with tagged commands or blocks of data, using the Virtual Channel ID field of the header for packets targeted at different peripherals.

Virtual Channel (VC) is a part of Data Identification (DI[7...6]) structure and it is used to address where a packet is wanted to send from the MCU. Bits of the Virtual Channel (VC) are

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illustrated for reference purposes below.

AXS15260D-S1 only support VC code=00, package with other VC code(01/10/11) will be filter out.

DI							WC(Least Significant Byte)							WC(Most Significant Byte)							ECC										
39hex							01hex							00hex							15hex										
1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0
B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	0	1	2	3	4	5	6	7
L							M	L							M	L							M	L						M	
S							S	S							S	S							S	S					S		
B							B	B							B	B							B	B					B		

Figure: Virtual channel on the packet head

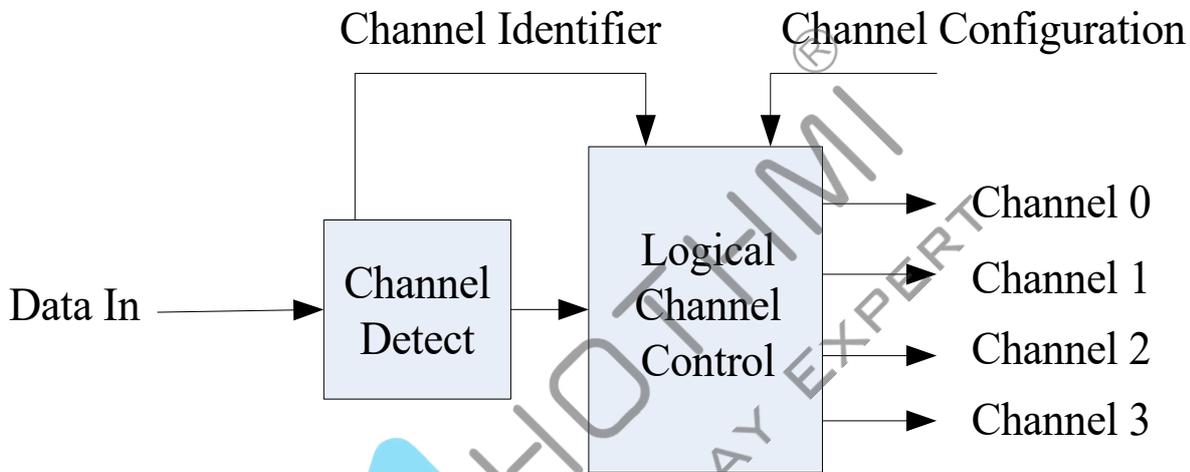


Figure: Virtual channel block diagram (receiver case)

Data Type (DT)

Data Type (DT) is a part of Data Identification (DI[5...0]) structure and it is used to define a type of the used data on a packet.

Bits of the Data Type (DT) are illustrated for reference purposes below.

DI							WC(Least Significant Byte)							WC(Most Significant Byte)							ECC										
39hex							01hex							00hex							15hex										
1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0	
B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	0	1	2	3	4	5	6	7
L							M	L							M	L							M	L					M		
S							S	S							S	S							S	S					S		
B							B	B							B	B							B	B					B		

Figure: Data type on the packet head

This Data Type (DT) also defines what the used packet is: Short Packet (SPa) or Long Packet (LPa). Data Types (DT) are different from the MCU to the display module (or other devices) and vice versa. These Data Type (DT) are defined on tables below.

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From the MCU to the Display module		
Data Type(HEX)	Data Type(Binary)	Description
01h	00 0001	Sync Event, V Sync Start
11h	01 0001	Sync Event, V Sync End
21h	10 0001	Sync Event, H Sync Start
31h	11 0001	Sync Event, H Sync End
08h	00 1000	End of Transmission (EoT)packet
03h	00 0011	Generic Short WRITE, no parameters
13h	01 0011	Generic Short WRITE, 1 parameters
23h	10 0011	Generic Short WRITE, 2 parameters
04h	00 0100	Generic READ, no parameters
14h	01 0100	Generic READ, 1 parameters
24h	10 0100	Generic READ, 2 parameters
05h	00 0101	DCS WRITE, no parameters
15h	01 0101	DCS WRITE, 1 parameters
06h	00 0110	DCS READ, no parameters
37h	11 0111	Set Maximum Return Packet Size
09h	00 1001	Null Packet, no data
19h	01 1001	Blanking Packet, no data
29h	10 1001	Generic Long Write
39h	11 1001	DCS Long Write/Write_LUT Command packet
3Eh	11 1110	Packet Pixel Stream, 24-bit RGB, 8-8-8 Format
0Eh	001110	Packed Pixel Stream, 16-bit RGB, 5-6-5 Format
1Eh	011110	Packed Pixel Stream, 18-bit RGB, 6-6-6 Format
2Eh	101110	Loosely Packed Pixel Stream, 18-bit RGB, 6-6-6 Format

Table: Data type from the MCU to the display module

From the Display module to the MCU		
Data Type(HEX)	Data Type(Binary)	Description
1Ch	01 1100	DCS Long Read Response
21h	10 0001	DCS Short Read Response, 1 Byte returned
22h	10 0010	DCS Short Read Response, 2 Byte returned
1Ah	011010	Generic Long READ Response
11h	01 0001	Generic Short Read Response, 1 Byte returned
12h	01 0010	Generic Short Read Response, 2 Byte returned

Table: Data type from the display module to the MCU

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The receiver will ignore other Data Type (DT) if they are not defined on tables above. Host send “Generic Read” data type, AXS15260D-S1 will return Generic Read package to Host.

Packet data on the short packet

Packet Data (PD) of the Short Packet (SPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Short Packet (SPa) is wanted to send. Packet Data (PD) of the Short Packet (SPa) consists of 2 data bytes: Data 0 and Data 1. Packet Data (PD) sending order is that Data 0 is sent in the first and the Data 1 is sent in the last. Bits of Data 1 are set to 00h, if the information length is 1 byte. Packet Data (PD) of the Short Packet (SPa), when the length of the information is 1 or 2 bytes are illustrated for reference purposes below.

DI								Data 0								Data 1								ECC											
15hex								35hex								01hex								1Ehex											
1	0	1	0	1	0	0	0	1	0	1	0	1	1	0	0	1	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0				
B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B				
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	0	1	2	3	4	5	6	7				
L								M	L								M	L								M	L								M
S								S	S								S	S								S	S								S
B								B	B								B	B								B	B								B

Figure: Packet data on the short packet, 2 bytes information

Packet Data (PD) information:

- Data 0: 10hex
- Data 1: 00hex (Null)

DI								Data 0								Data 1								ECC											
05hex								10hex								00hex								2Chex											
1	0	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1	0	0				
B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B	B				
0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	0	1	2	3	4	5	6	7				
L								M	L								M	L								M	L								M
S								S	S								S	S								S	S								S
B								B	B								B	B								B	B								B

Figure: Packet data on the short packet, 1 bytes information

Word count on the long packet

Word Count (WC) of the Long Packet (LPa) is defined after Data Type (DT) of the Data Identification (DI) has indicated that Long Packet (LPa) is wanted to send. Word Count (WC) indicates a number of the data bytes of the Packet Data (PD) what is wanted to send after Packet Header (PH) versus Packet Data (PD) of the Short Packet (SPa) is placed in the Packet Header (PH). Word Count (WC) of the Long Packet (LPa) consists of 2 bytes.

These 2 bytes of the Word Count (WC) sending order is that the Least Significant (LS) Byte is sent in the first and the Most Significant (MS) Byte is sent in the last.

Word Count (WC) of the Long Packet (LPa) is illustrated for reference purposes below.

DI								WC(Least Significant Byte)								WC(Most Significant Byte)								ECC							
39hex								01hex								00hex								15hex							
1	0	0	1	1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0	0	0

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- $P2 = D0 \wedge D2 \wedge D3 \wedge D5 \wedge D6 \wedge D9 \wedge D11 \wedge D12 \wedge D15 \wedge D18 \wedge D20 \wedge D21 \wedge D22$
- $P1 = D0 \wedge D1 \wedge D3 \wedge D4 \wedge D6 \wedge D8 \wedge D10 \wedge D12 \wedge D14 \wedge D17 \wedge D20 \wedge D21 \wedge D22 \wedge D23$
- $P0 = D0 \wedge D1 \wedge D2 \wedge D4 \wedge D5 \wedge D7 \wedge D10 \wedge D11 \wedge D13 \wedge D16 \wedge D20 \wedge D21 \wedge D22 \wedge D23$

P7 and P6 are set to '0' because Error Correction Code (ECC) is based on 64 bit value ([D63...0]), but this implementation is based on 24 bit value (D[23...0]). Therefore, there is only needed 6 bits (P[5...0]) for Error Correction Code (ECC).

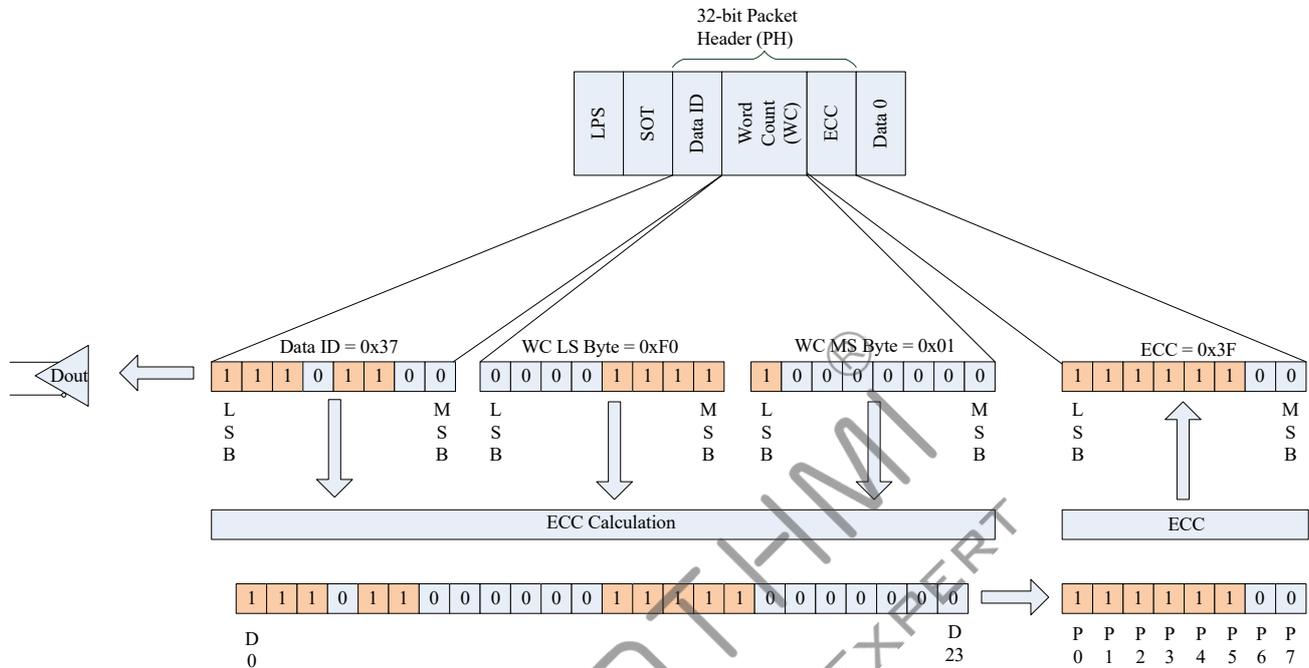


Figure: 24-bit ECC generation on TX side (Example)

Packet footer on the long packet

Packet Footer (PF) of the Long Packet (LPa) is defined after the Packet Data (PD) of the Long Packet (LPa). The Packet Footer (PF) is a checksum value what is calculated from the Packet Data of the Long Packet (LPa).

The checksum is using a 16-bit Cyclic Redundancy Check (CRC) value which is generated with a polynomial $X^{16}+X^{12}+X^5+X^0$ as it is illustrated below.

Polynomial: $X^{16}+X^{12}+X^5+X^0$

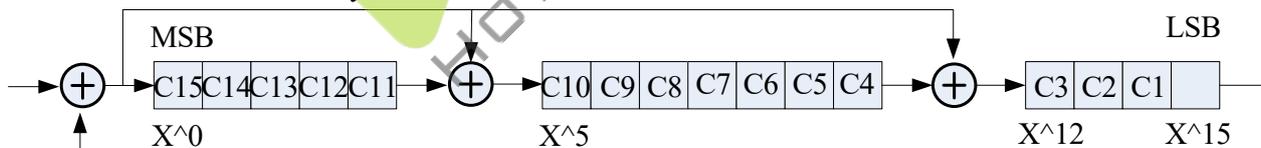


Figure: 16-bit cyclic redundancy check (CRC) calculation

The 16-bit Cyclic Redundancy Check (CRC) generator is initialized to FFFFh before calculations. The Most Significant Bit (MSB) of the data byte of the Packet Data (PD) is the first bit what is inputted into the 16-bit Cyclic Redundancy Check (CRC). The receiver is calculated own checksum value from received Packet Data (PD). The receiver compares own checksum and the Packet Footer (PF) what the transmitter has sent. The received Packet Data (PD) and Packet Footer (PF) are correct if the own checksum of the receiver and Packet Footer (PF) are equal and vice versa the received Packet Data (PD) and Packet Footer (PF) are not correct if the own checksum of the receiver and Packet Footer (PF) are not equal.

5.3.4.2 Packet transmissions

Packet from the MCU to the display module

Display Command Set (DCS), which is defined on chapter “Instructions” is used from the MCU to the display module. This Display Command Set (DCS) is always defined on the Data 0 of the Packet Data (PD), which is included in Short Packet (SPa) and Long packet (LPa) as these are illustrated below.

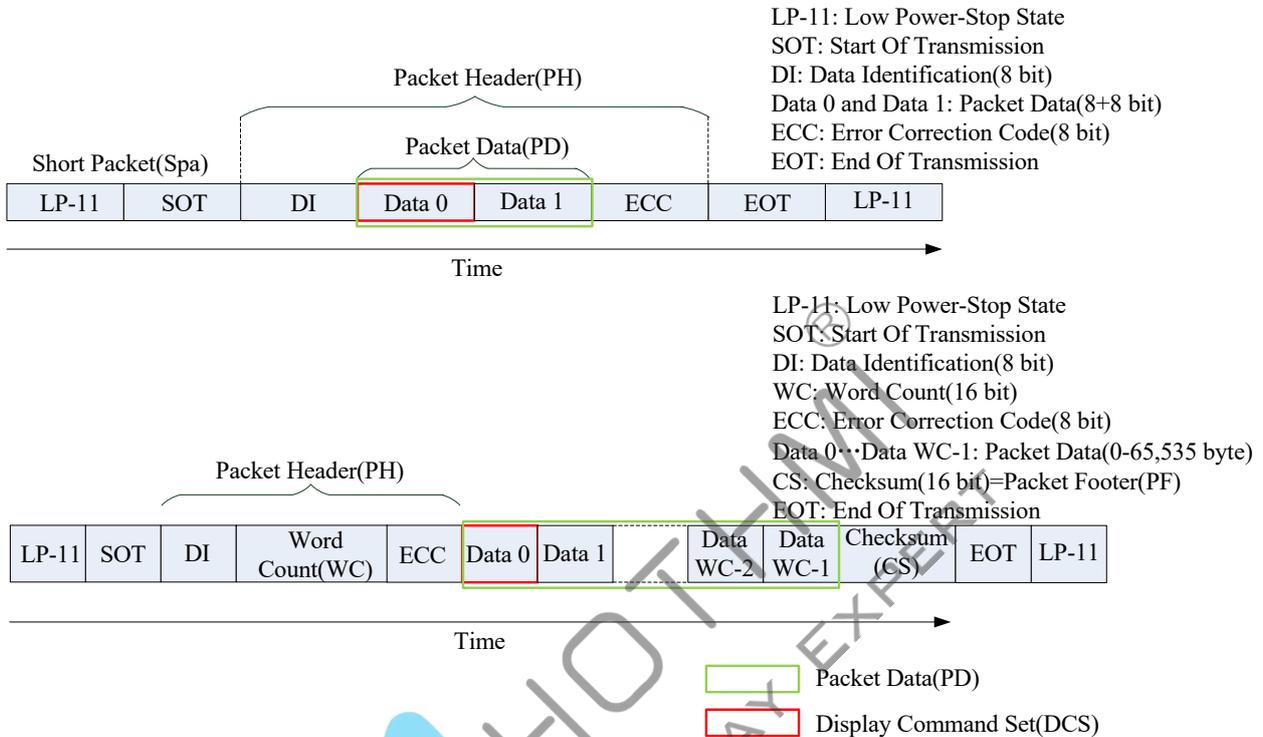


Figure: DCS on the short packet and long packet

Packet from the display module to the MCU

Used packet types

The display module is always using Short Packet (SPa) or Long Packet (LPa), when it is returning information to the MCU after the MCU has requested information from the Display Module. This information can be a response of the Display Command Set (DCS).

The used packet type is defined on Data Type (DT).

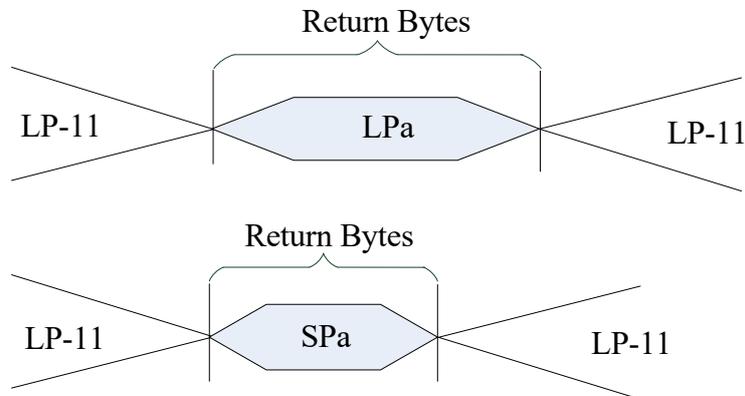


Figure: Return bytes on single packet

5.3.5 Customer-defined generic read data type format

The short packet of Data Type 14h (Generic READ, 1 parameters) specifies the register content for read and the Nth parameter that will begin reading. After Data Type 14h is received, BTA is executed. Then, the Nth parameter becomes the first data, and the number of data of WC (word count) value is output.

Packet Structure(processor → peripheral)

	Data Type 24h	Manufacturer Command	Start Parameter N	ECC	
--	------------------	-------------------------	----------------------	-----	--

Low Power Data Transfer(peripheral → processor)

	Data Type 1Ah	WC 0	WC 1	WC 2	1th Parameter	2th Parameter		Nth Parameter	CRC 0	CRC 1	
--	------------------	---------	---------	---------	------------------	------------------	--	------------------	----------	----------	--

Figure: Generic read data type format

5.3.6 MIPI video parameter

In the MIPI video mode, the frame is transmitted from the host processor to a display module as a sequence of pixels, with each horizontal line of the image data sent as a group of consecutive pixels.

Vsync (VS) indicates the beginning of each frame of the displayed image.

Hsync (HS) signals the beginning of each horizontal line of pixels.

Each pixel value (16-, 18-, or 24-bit data) is transferred from the host processor to the display module during one pixel period. The rising edge of PCLK is used by the display module to capture pixel data. Since PCLK runs continuously, control signal DE is required to indicate when valid pixel data is being transmitted on the pixel data signals.

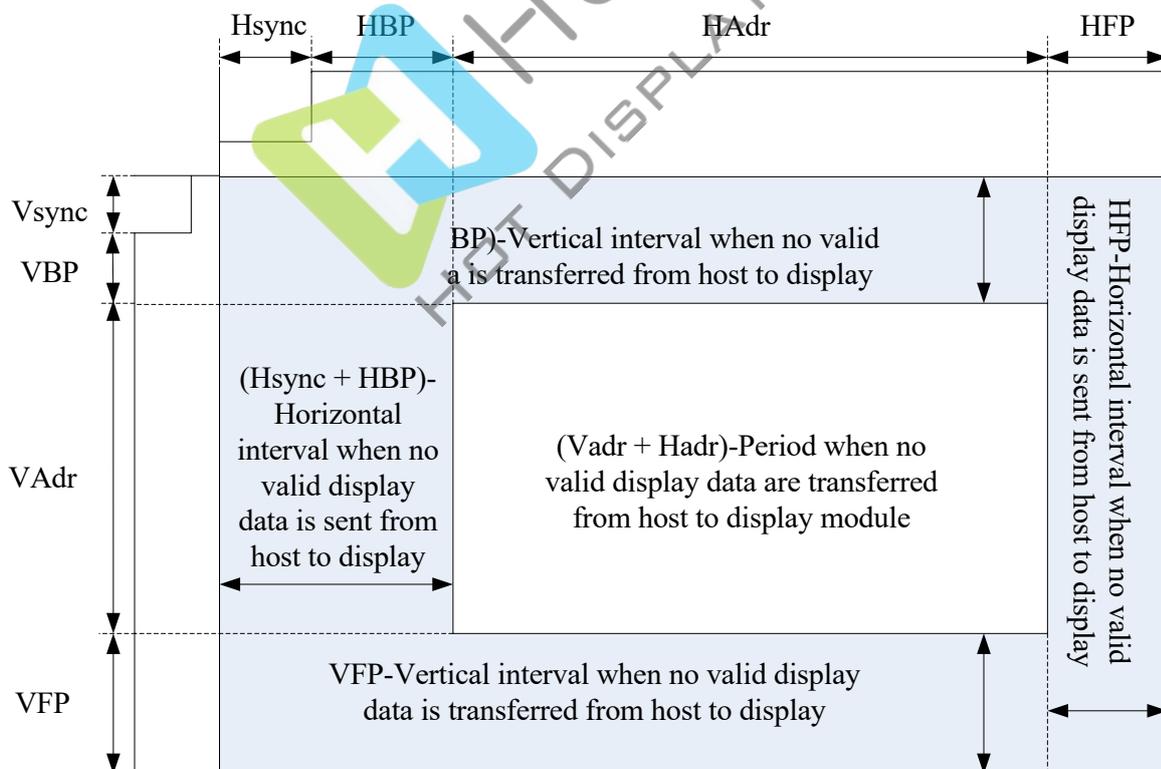


Figure 6.2.6.1 define timing parameter for MIPI video operation.

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(Resolution for 320 horizontal x 480 vertical display with Frame-Rate of 60 Hz)

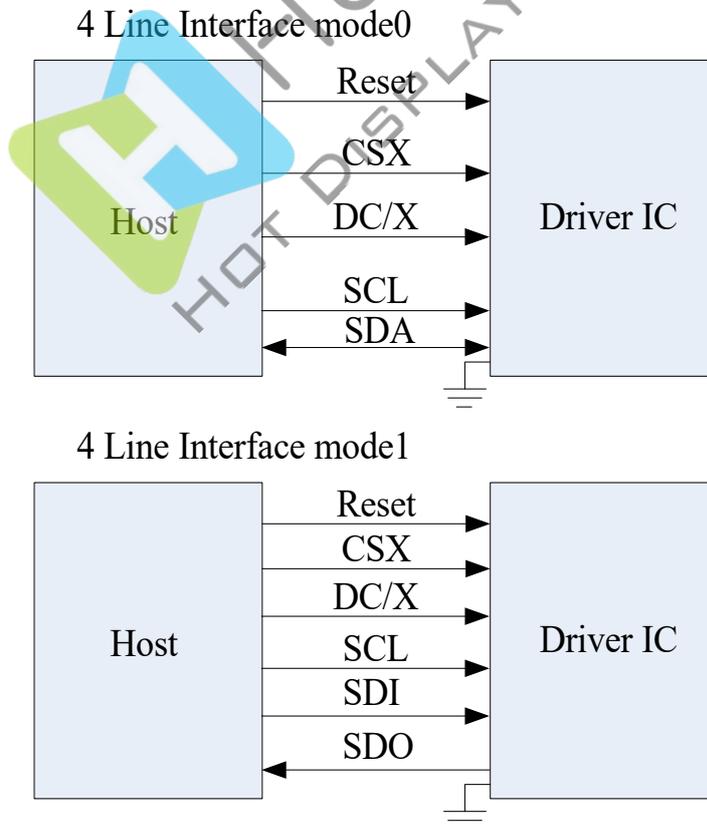
Parameters	Symbols	Min.	Typ	Max.	Unit
Horizontal Synchronization	Hsync	2	2	-	PCLK
Horizontal Back Porch	HBP	2	60	-	PCLK
Horizontal Front Porch	HFP	2	60	-	PCLK
Hsync+ HBP+ HFP	-	6	122	-	PCLK
Horizontal Address (Display area)	HAdr	-	320	-	PCLK

5.4 Serial Interface (SPI)

5.4.1 4-Line Interface

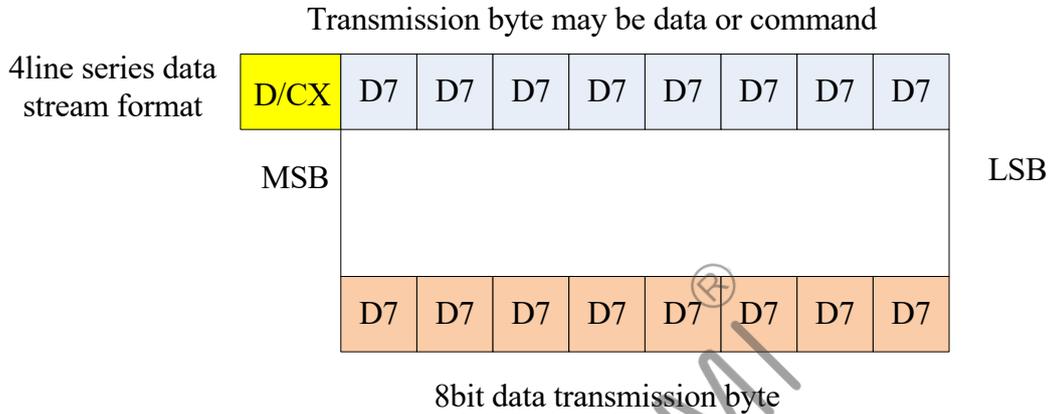
Connect Pin: DIN_SDA(SDI), DIN_SDA_DUAL(SDO), RS(D/CX), SCL, CSX, RSTN

The Serial Peripheral Interface (SPI) is selected by setting the IM[3:0] pins as “1101” level. The chip select pin (CSX), the serial transfer clock pin (SCL), the display data/command selection (D/CX), the serial data input/output pin (SDA or SDI/SDO) are used in SPI mode. The ID pin sets the least significant bit of the identification code. The DB[23:0] pins, which are not used, must be tied to GND

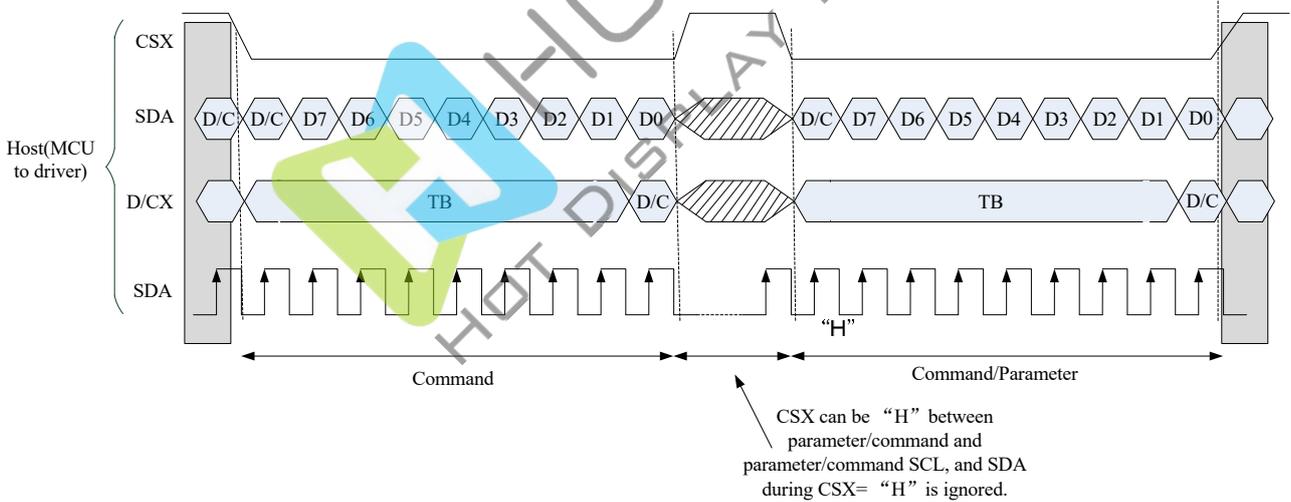


5.4.1.1 Write Sequence

The write mode of the interface means the host writes commands and data to AXS15260D-S1. The 4-lines serial data packet contains a data/command and a transmission byte. If D/CX is “low”, the transmission byte is interpreted as a command byte. If D/CX is “high”, the transmission byte is interpreted as a parameter. The transmission byte is stored in the display data RAM (Memory write command), or command register as parameter.



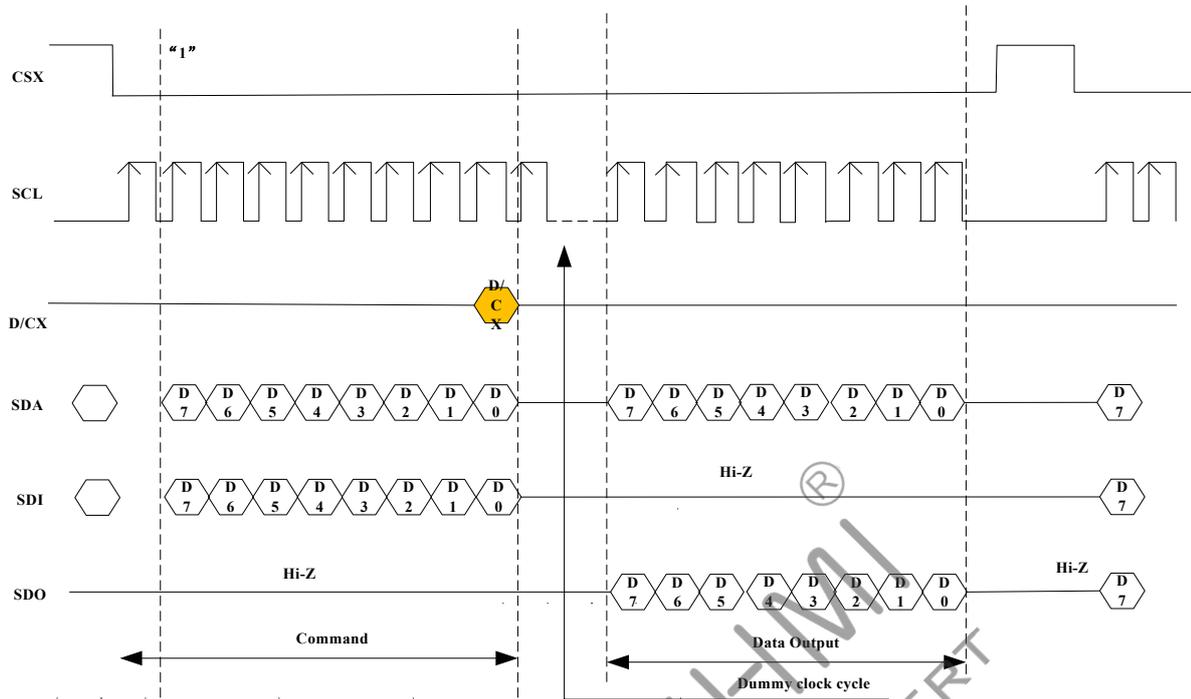
The host drives the CSX pin to low and the MSB data bit (D7) is set on SDA by the host. On the next falling edge of SCL the next bit (D6) is set on SDA. If the optional D/CX signal is used, a byte is eight read cycle long. The 4-line serial interface writes sequence described in the Figure as below.



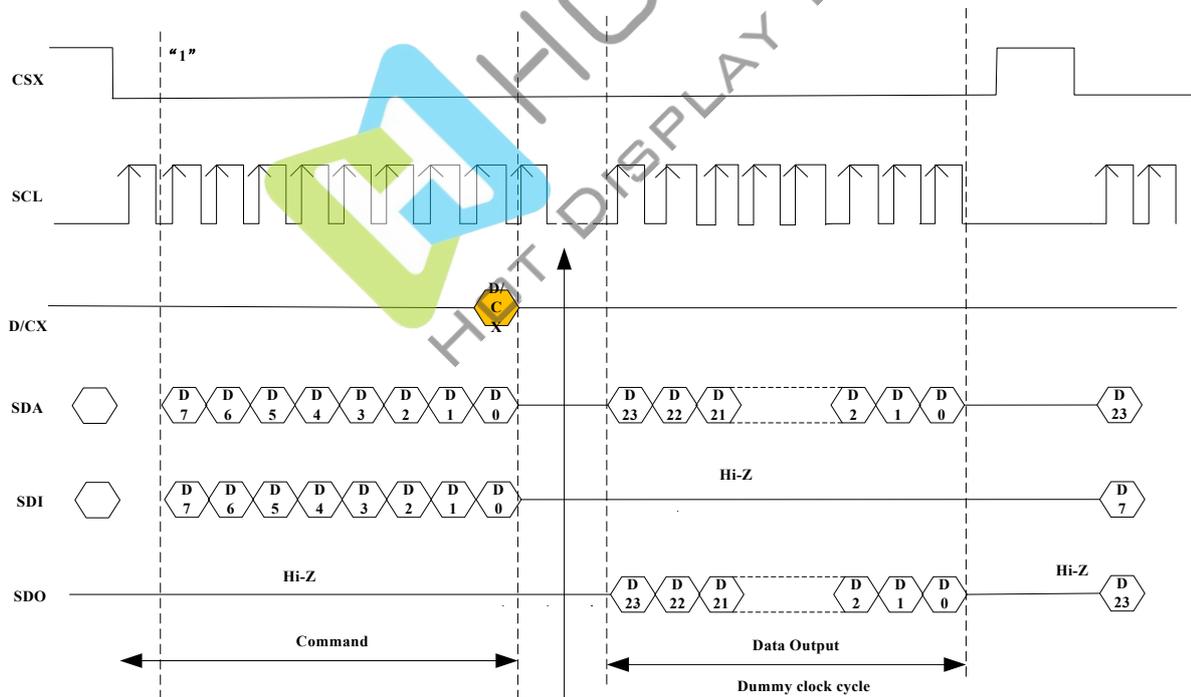
5.4.1.2 Read Sequence

The read mode of the interface means that the micro controller reads register value from the driver. To achieve read function, the micro controller first has to send a command (read ID or register command) and then the following byte is transmitted in the opposite direction. After that CSX is required to go to high before a new command is send (see the below figure). The driver samples the SDA (input data) at rising edge of SCL, but shifts SDA (output data) at the falling edge of SCL. Thus the micro controller is supported to read at the rising edge of SCL.

5.4.1.2.1 4-line serial protocol (8-bit read, cr_spi_rd_en=1):

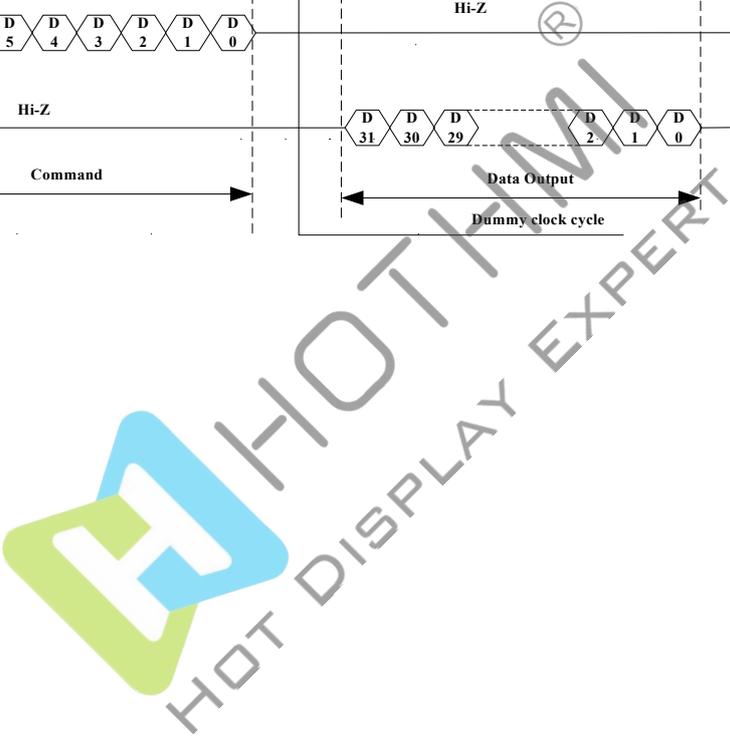
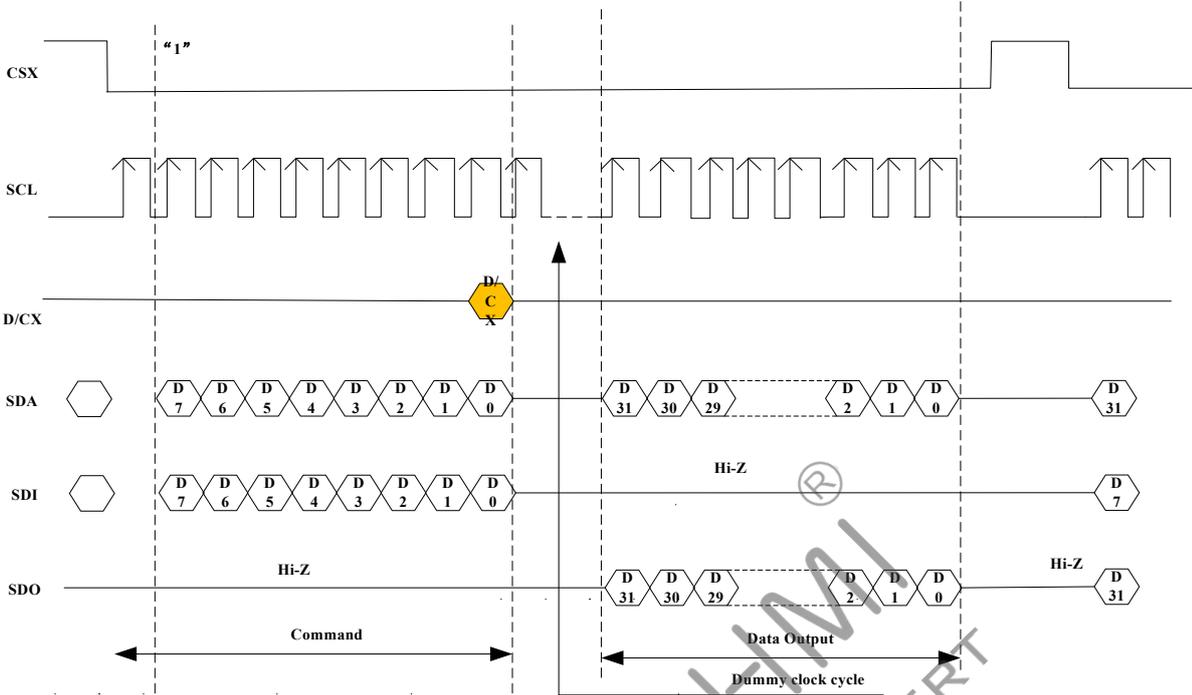


5.4.1.2.2 4-line serial protocol (24-bit read, cr_spi_rd_en=1)



AXS15260D-S1

5.4.1.2.3 4-line serial protocol (32-bit read, cr_spi_rd_en=1)



5.5 RGB Interface

5.5.1 RGB Color Format

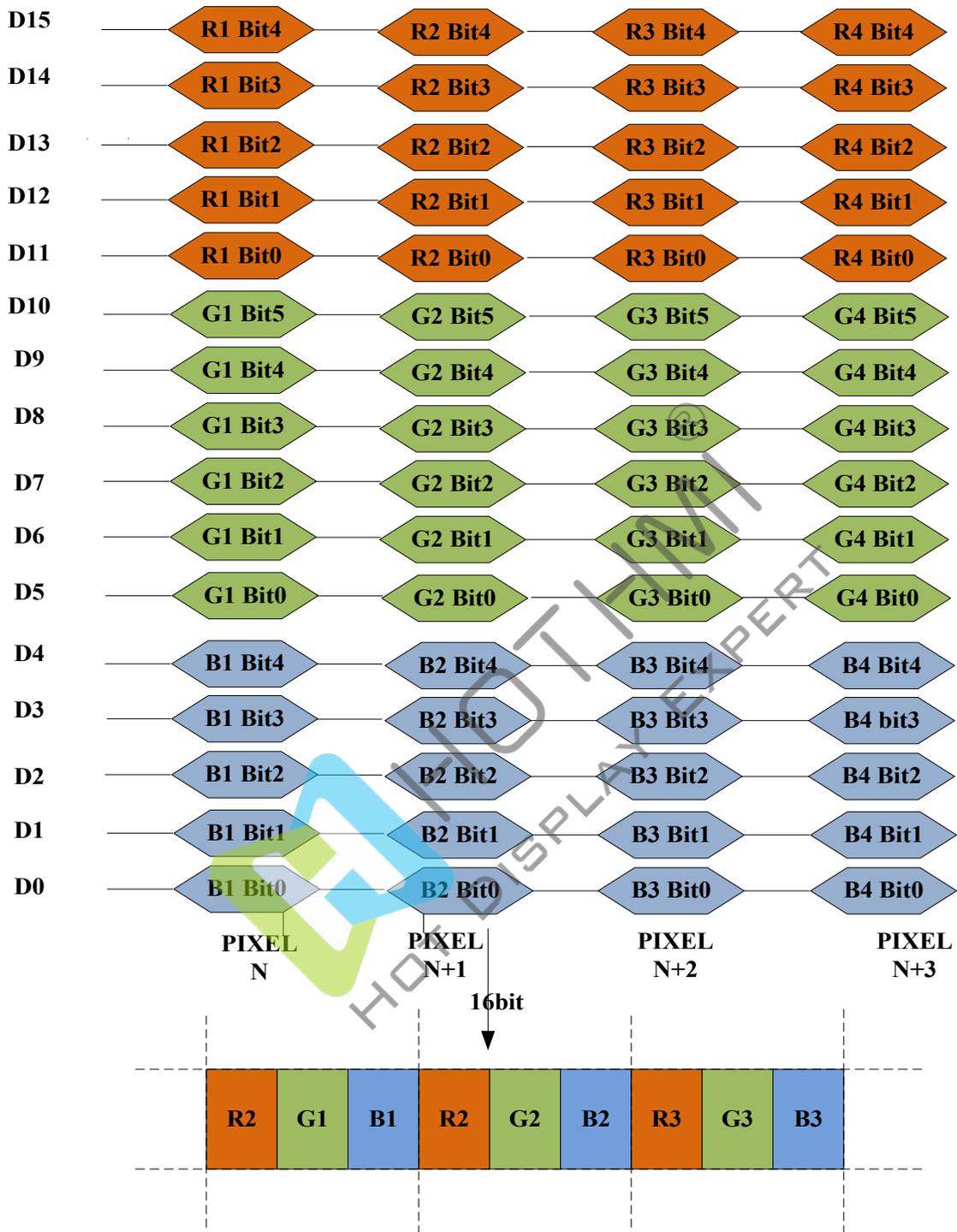
Connect Pin:DB[15/17/23:0],VSYNC_QSPI_DIN2,HSYNC,DE_QSPI_DIN3,PCLK

AXS15260D-S1 supports two kinds of RGB interface, DE mode , and 16bit/18bit/24bit data format. When DE mode is selected and the VSYNC, HSYNC, DOTCLK, DE, DB[15/17/23:0] pins can be used; When using RGB interface, only serial interface can be selected. IM [3:0] as “1110”。



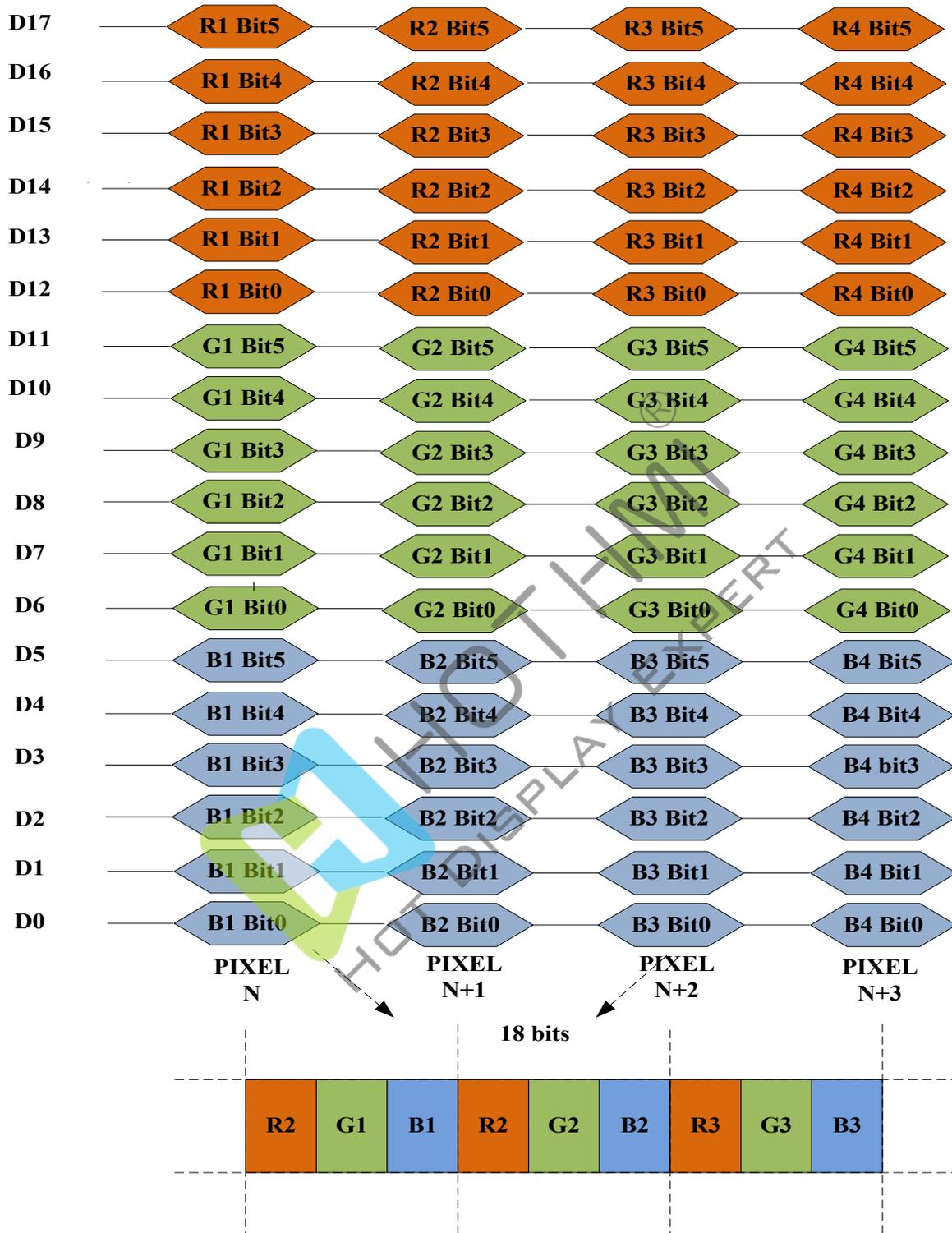
AXS15260D-S1

5.5.1.1 Write data for 16-bit/pixel (RGB 5-6-5-bit input)65K-Colors



AXS15260D-S1

5.5.1.2 Write data for 18-bit/pixel (RGB 6-6-6-bit input)262K-Colors



AXS15260D-S1

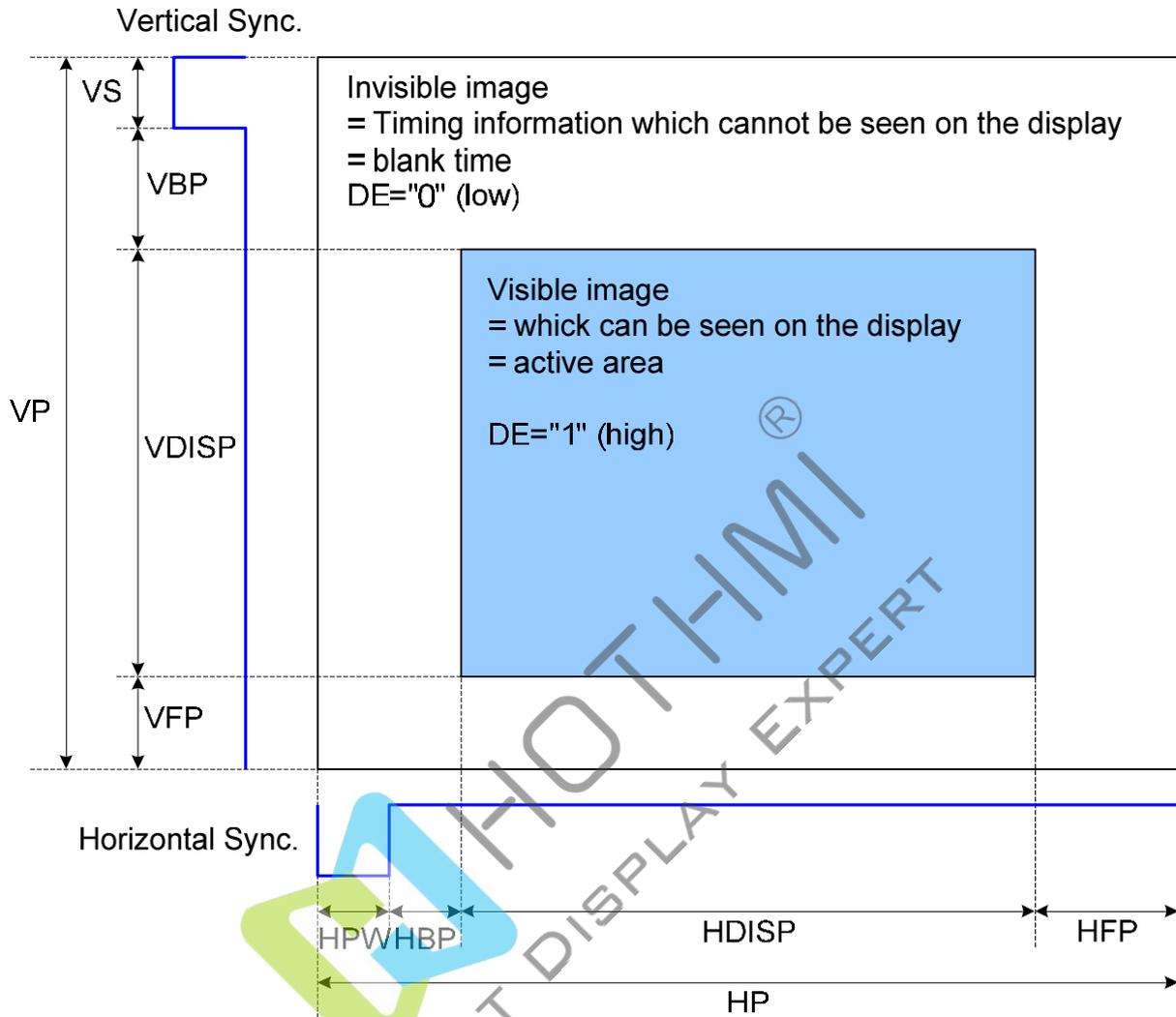
5.5.1.3 Write data for 24-bit/pixel (RGB 8-8-8-bit input)16.7M-Colors



5.5.2 RGB Interface Definition

AXS15260D-S1

The display operation via the RGB interface is synchronized with the VSYNC, HSYNC, and DOTCLK signals. The data can be written only within



the specified area with low power consumption by using window address function. The back porch and front porch are used to set the RGB interface timing.

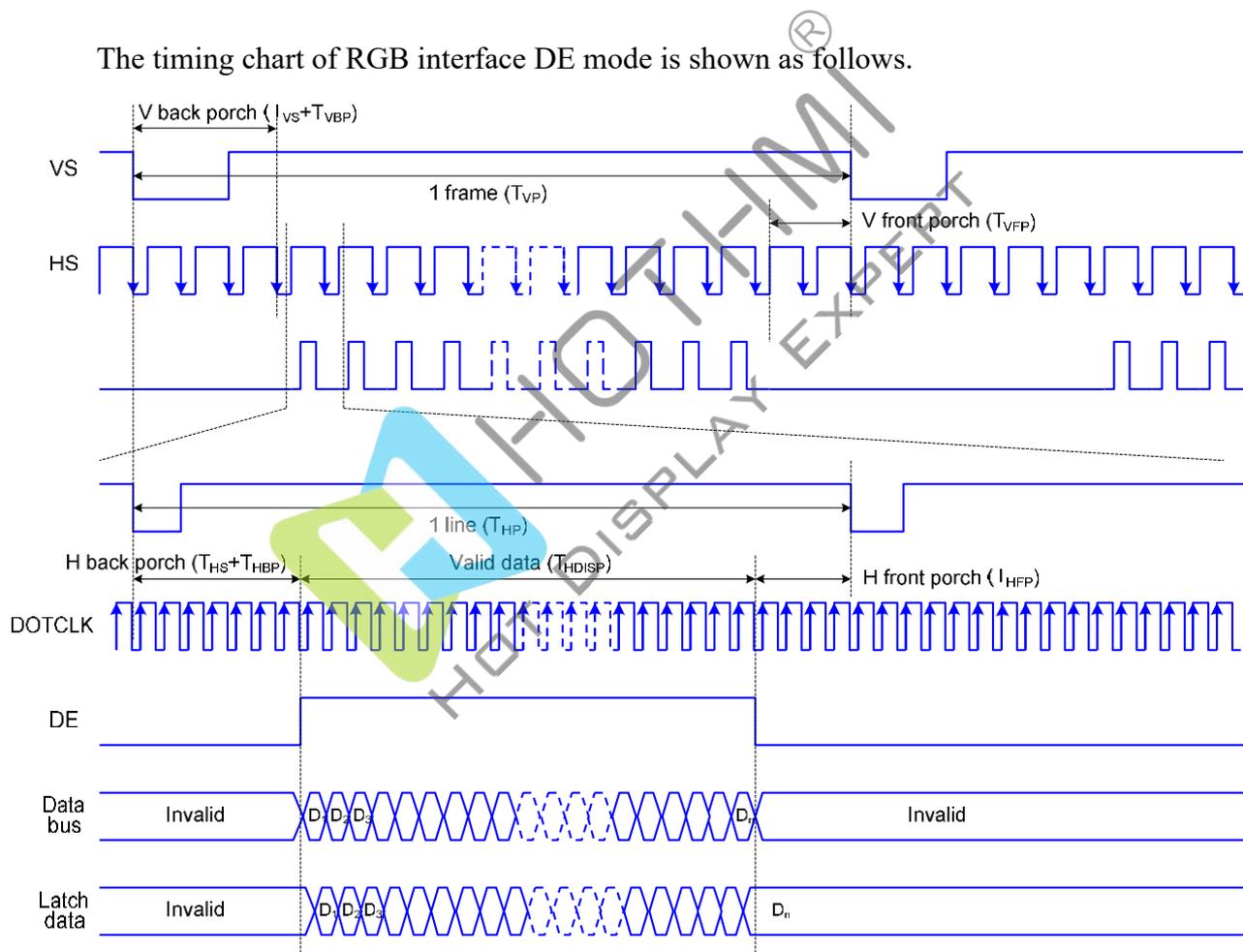
DRAM Access Area by RGB Interface

Please refer to the following table for the setting limitation of RGB interface signals.

Parameter	Symbol	Min.	Typ.	Max.	Unit
Horizontal Sync. Width	hpw	-	2	hpw+hbp=75	Clock
Horizontal Sync. Back Porch	hbp	-	30		Clock
Horizontal Sync. Front Porch	hfp	-	30	-	Clock
Vertical Sync. Width	vs	-	2	-	Line
Vertical Sync. Back Porch	vbp	-	254		Line
Vertical Sync. Front Porch	vfp	-	10	-	Line

5.5.3 RGB Interface Timing

The timing chart of RGB interface DE mode is shown as follows.



Note: The setting of front porch and back porch in host must match that in IC as this mode.

VSYNC, HSYNC, and DOTCLK signals must be supplied during a display operation period.

In RGB interface mode, the panel controlling signals are generated from DOTCLK, not the internal clock generated from the internal oscillator.

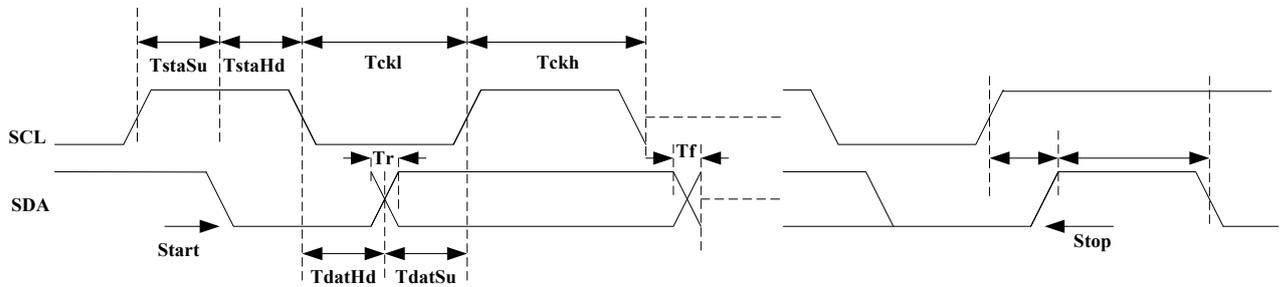
When switching between the internal operation mode and the external display interface operation mode, follow the sequences below in setting instruction.

In RGB interface mode, the front porch period continues until the next VSYNC input is

detected after drawing one frame. In RGB interface mode, a RAM address is set in the address counter every frame on the falling edge of VSYNC.

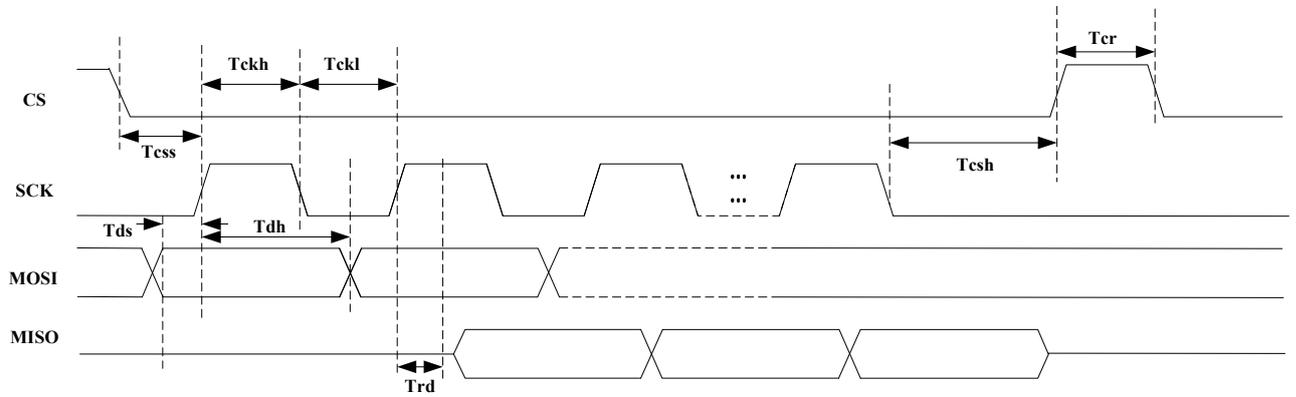
5.6 Touch part interface

5.6.1 I2C Interface



Parameter	Symbol	Min.	Typ	Max.	Unit
Working Frequency	F_{clk}	20	-	400	Khz
I2C Clock Low	T_{CKL}	1300	-	-	ns
I2C Clock High	T_{CKH}	600	-	-	ns
I2C Clock and Data rising time	T_r	-	-	300	ns
I2C Clock and Data falling time	T_f	-	-	300	ns
I2C Data hold time	T_{DatHd}	0	-	-	ns
I2C Data setup time	T_{DatSu}	100	-	-	ns
I2C Start Condition hold time	T_{StaHd}	600	-	-	ns
I2C Start Condition setup time	T_{StaSu}	600	-	-	ns
I2C Stop Condition setup time	T_{StpSu}	600	-	-	ns
I2C Bus free time	$T_{BusFree}$	1300	-	-	ns

5.6.2 SPI Interface



SPI Timing

Parameter	Symbol	Min.	Typ	Max.	Unit
SCK Frequency	f_{SCK}	-	-	18	Mhz
CS Set-up Time	t_{CSS}	200	-	-	ns
CS Hold Time	t_{CSH}	200	-	-	ns
CS Recovery Time	t_{CR}	1	-	-	ns
SCK clock High Time	t_{CKH}	27.8	-	-	ns
SCK clock Low Time	t_{CKL}	27.8	-	-	ns
Data Output Delay Time	t_{RD}	-	-	-	ns
Input Data Set-up Time	t_{DS}	25	-	-	ns
Input Data Hold Time	t_{DH}	25	-	-	ns

5.7 Display Reference Clock Function

The AXS15260D-S1 provides a function to decide internal oscillator for display clock reference of driver IC.

Relationship between Liquid Crystal Driver Duty and the Frame Frequency

The formula below is used to calculate the relationship between the liquid crystal driver duty and the frame frequency. The frame frequency is determined by setting the 1H period adjustment (RTN) bit.

RTN setting for 1H period:

Step1: To decide real one line period in Command Mode:

$$RTN = 1H(\text{period}) = \frac{F_{osc} - 5\%}{(\text{Line} + BP + FP) * \text{FrameRate}(\text{Hz})}$$

$$RTN = 1H(\text{period}) = \frac{F_{pll} - 5\%}{(\text{Line} + BP + FP) * \text{FrameRate}(\text{Hz})} (\mu\text{s}) \text{ (Note.1, Note.2, Note.3)}$$

RTN: Number of clocks per line.

Line: Display Line Number

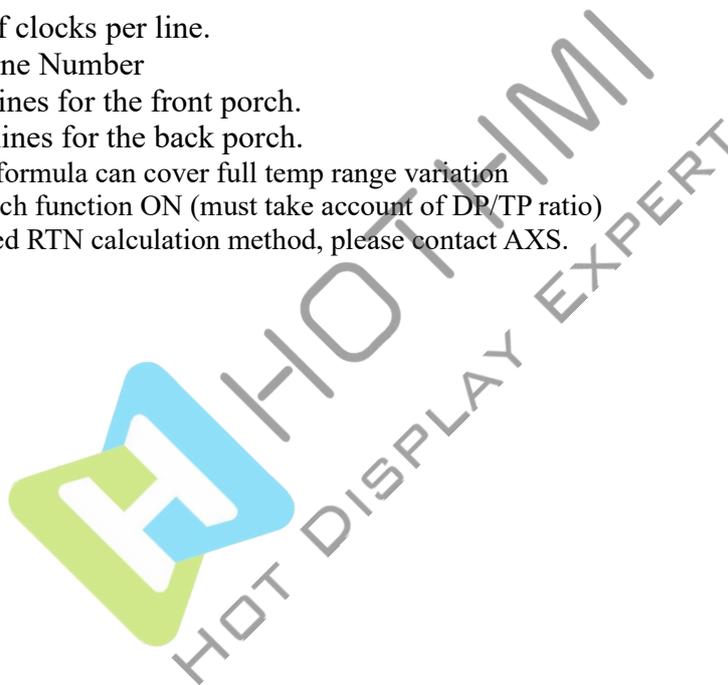
FP: Number of lines for the front porch.

BP: Number of lines for the back porch.

Note.1: The RTN formula can cover full temp range variation

Note.2: When Touch function ON (must take account of DP/TP ratio)

Note.3: For detailed RTN calculation method, please contact AXS.



5.8 Gamma Function

The structure of grayscale amplifier is shown as below. The 30 voltage levels between VSPR/VSNR and GND determined by the gradient adjustment register, the reference adjustment register, the amplitude adjustment register and the micro-adjustment register.

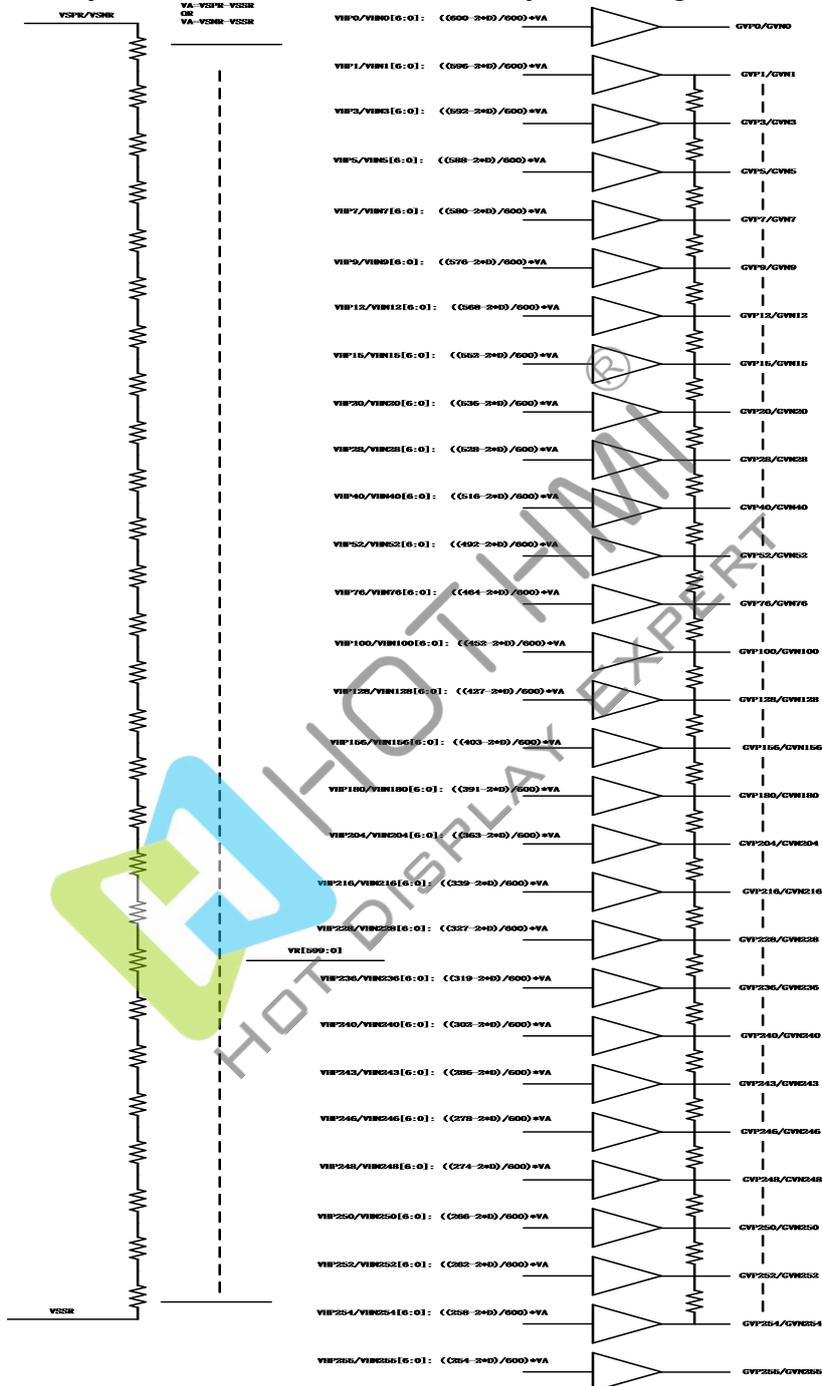


Figure: Gamma Architecture for AXS15260D-S1

5.9 Reset Function

The RESET function of AXS15260D-S1 is triggered by a RESX input. After reset function triggered, the AXS15260D-S1 enter a reset period, and the duration of this period must be at least 5ms. During this period, the AXS15260D-S1 and its power circuit will be initialized.

Initial States of Output Pins

The following table represents the output pins and its initial state.

Output Pins	Initial State
S<810:1>	GND
SX<480:1>	GND
VCOM	Disabled (GND level output)
GOUT_L[17:1], GOUT_R[17:1]	Disabled (GND level output)
LED_PWM	Disabled (GND level output)
VGH	Disabled
VGL	Disabled
VGHO	Disabled
VGLO	Disabled
VREF_TP	Disabled (Hi-z)
VCG_TP	Disabled (Hi-z)

5.10 Driver Operation Mode

AXS15260D-S1 driver can work in four operation modes of Reset State, Power Off state, Power On state and Display On State.

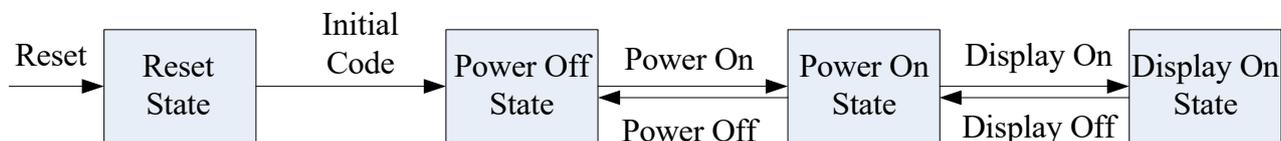
After reset, AXS15260D-S1 driver is in Reset state. In this state, all configurations are not initialized. Driver powers are not setup.

Initial code can be loaded from internal OTP or external flash or sent by host via MIPI interface. After the Initial code is loaded, AXS15260D-S1 driver enters Power Off state. AXS15260D-S1 driver is configured but powers are not up.

Power on command is sent from the Host. AXS15260D-S1 driver changes to Power On state on receiving power on command. All powers will be generated internally.

In Power on state, display on command can turn on the data path for display.

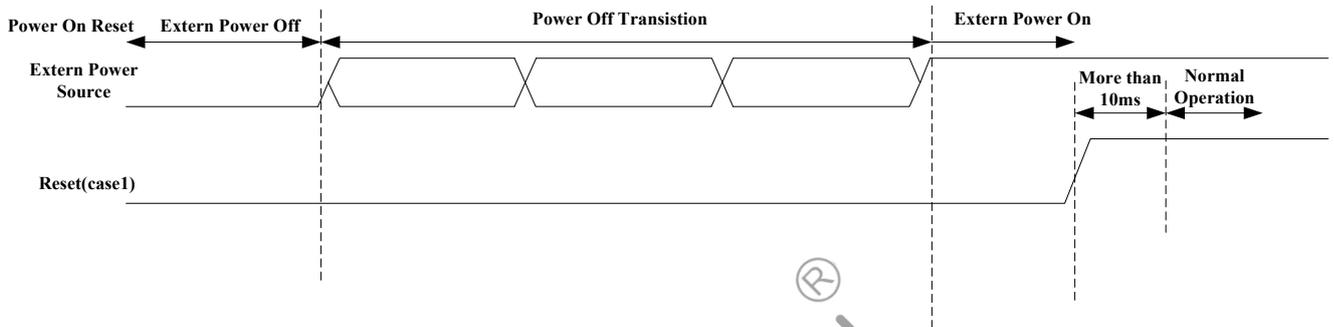
In Display on state, display off command can turn AXS15260D-S1 driver to Power On state and power off command can turn it to Power Off state.



5.10.1 Timing of Reset Pin

AXS15260D-S1 provides H/W pin to do driver IC initialization. For power-on reset, one-finger reset (Case1) methods can be applied to do driver IC initialization. The detailed H/W reset pin timing is shown as below.

Of the two methods, RESET(Case 2) is recommended.



H/W reset pin timing for power-on reset

5.11 Tear Effect Information

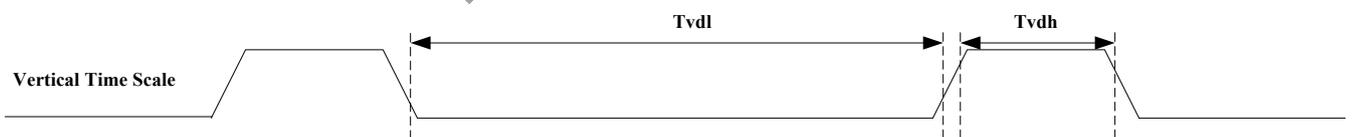
5.11.1 General

Tearing Effect line supplies to the MCU a Panel synchronization signal and this signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command

5.11.2 Tearing effect line models

The Tearing Effect line supplies to the MCU a Panel synchronization signal and this signal can be enabled or disabled by the Tearing Effect Line Off & On commands. The mode of the Tearing Effect Signal is defined by the Parameter of the Tearing Effect Line On command.

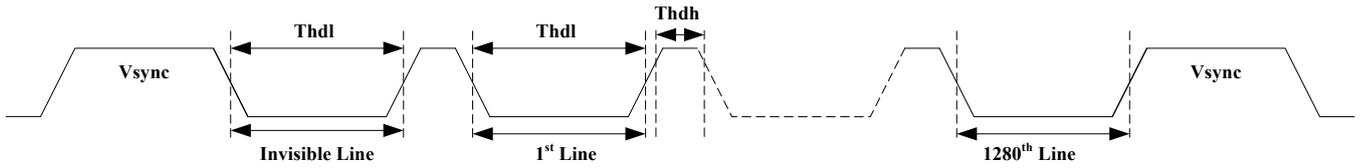
Mode1: The Tearing Effect Output signal consists of V-Sync information only:



$tvdh$ = The display panel is not updated from the Frame Memory.

$tvd1$ = The display panel is updated from the Frame Memory (except Invisible Line – see below).

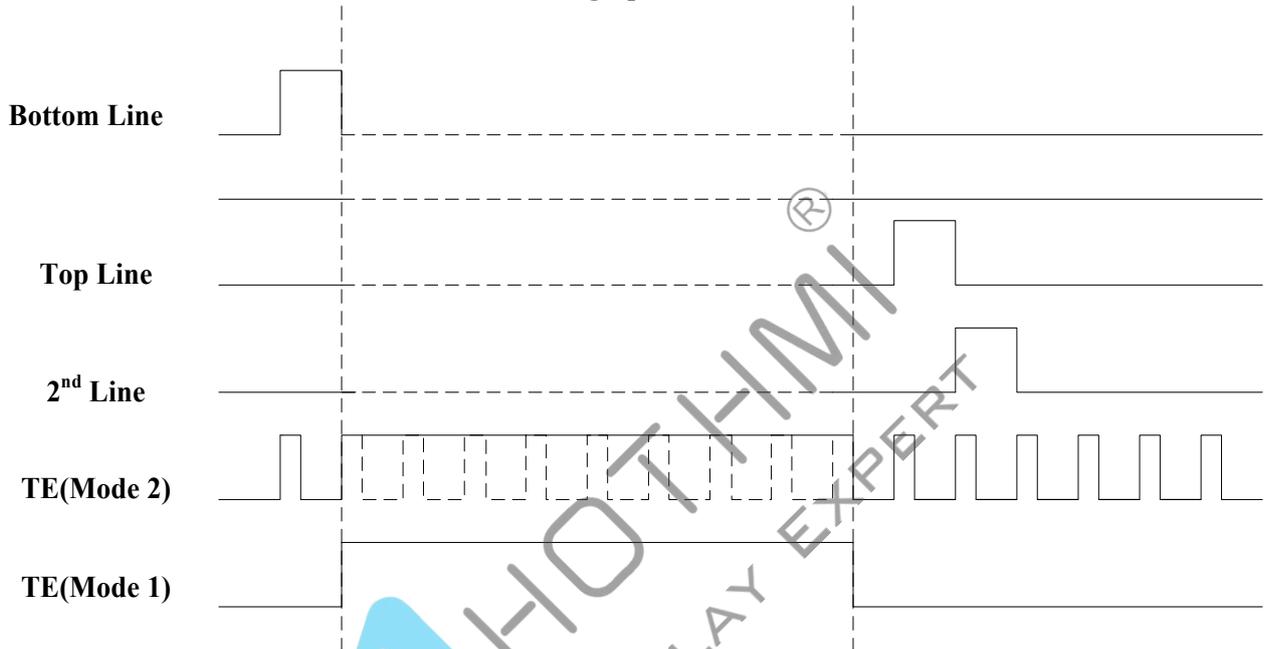
Mode 2 : The Tearing Effect Output signal consists of V-Sync and H-Sync information; There is one V-sync and 4 H-sync pulses per field:



t_{vdh} = The display panel is not updated from the Frame Memory.

t_{vdl} = The display panel is updated from the Frame Memory (except Invisible Line – see below).

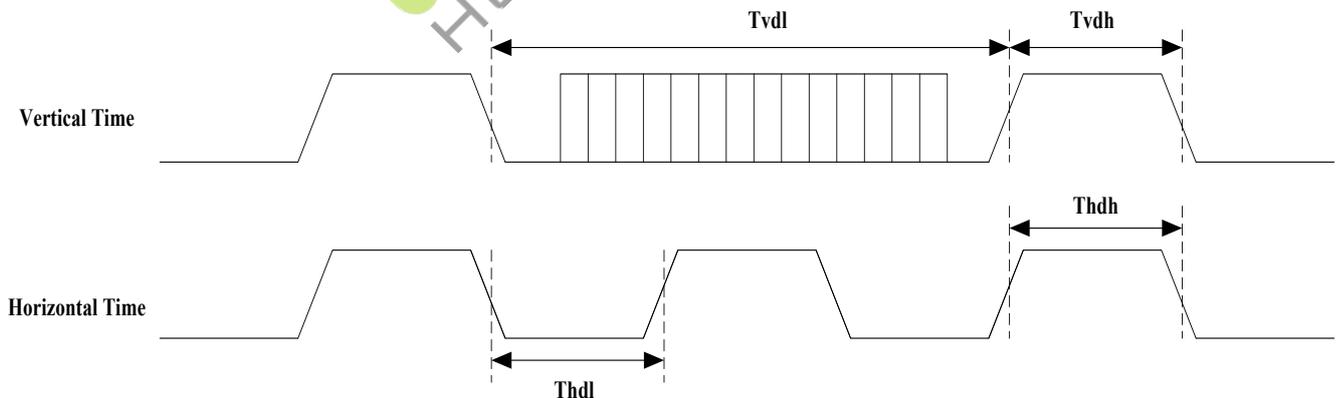
TE Line mode1 and Mode2 is shown as below graph:



Note: During Sleep In Mode, the Tearing Effect Output Pin is active Low.

5.11.2.1 Tearing effect line timing

The Tearing Effect signal is described below:

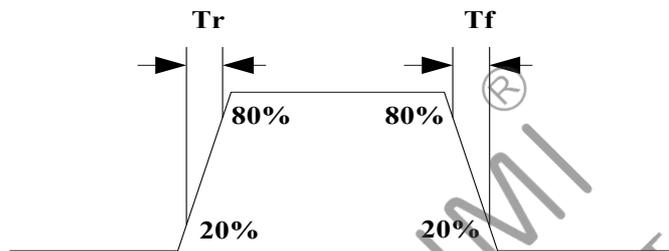


Symbol	Parameter	min	max	unit	description
--------	-----------	-----	-----	------	-------------

tvdl	Vertical Timing Low Duration	13	-	ms	
tvdh	Vertical Timing High Duration	1000	-	μ s	
thdl	Horizontal Timing Low Duration	16	-	μ s	
thdh	Horizontal Timing Low Duration	-	500	μ s	

Idle Mode Off/On

The TE signal rising and falling timing is described below:



5.12 OTP Programming Procedure

5.12.1 Power function description

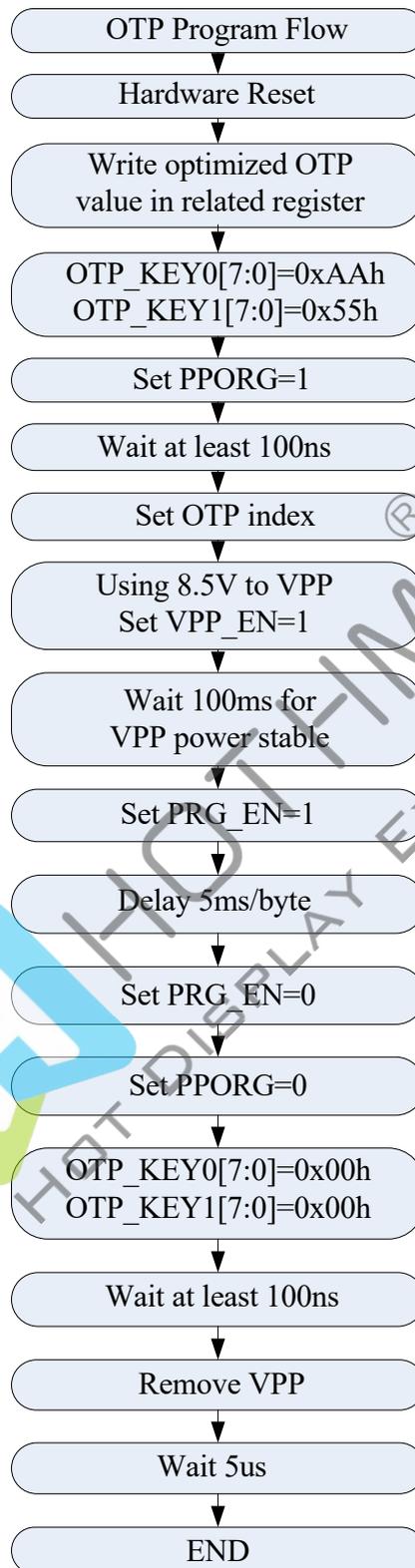
The OTP control signals control data reading and writing, only load once when reset. According to the request of the OTP, reset signal need delay at least 20ns to generate control signal. And signal transition should be less than 1ns.

STEP: Write the register parameters, then use index read all index, if both consistent, to write read content into the OTP. This method requires each register readout parameters contend is the same as written contend before. Each number of parameter is the same. And it may waste OTP resources if did not in byte. In order to prevent the wrong, the rest of resource as a reserve. The content behind can cover the front.

In the program, Write the index and parameters, matching read contend with register number, and loading the content behind in register.

In addition, you can also load OTP after reset release, and programming OTP by external interface generating timing.

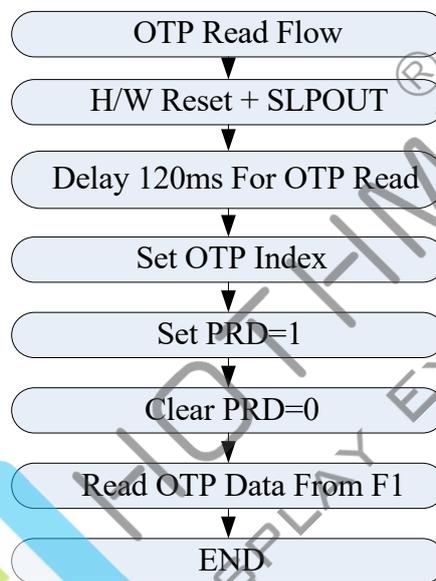
5.12.2 OTP program flow chart



Step	External Power OTP Program Sequence
1	Power on and reset the module
2	Write optimized OTP value in related register

3	OTP_KEY 0xAA 0x55
4	Set PPORG=1, wait 100ns
5	Set OTP index
6	Use 8.5V to VPP, Set VPP_EN=1, wait 100ms
7	Set PRG_EN=1, wait 5ms/byte
8	Set PRG_EN=0
9	Set PPORG=0, wait 100ns
10	OTP_KEY 0x00 0x00
11	Remove VPP, wait 5us

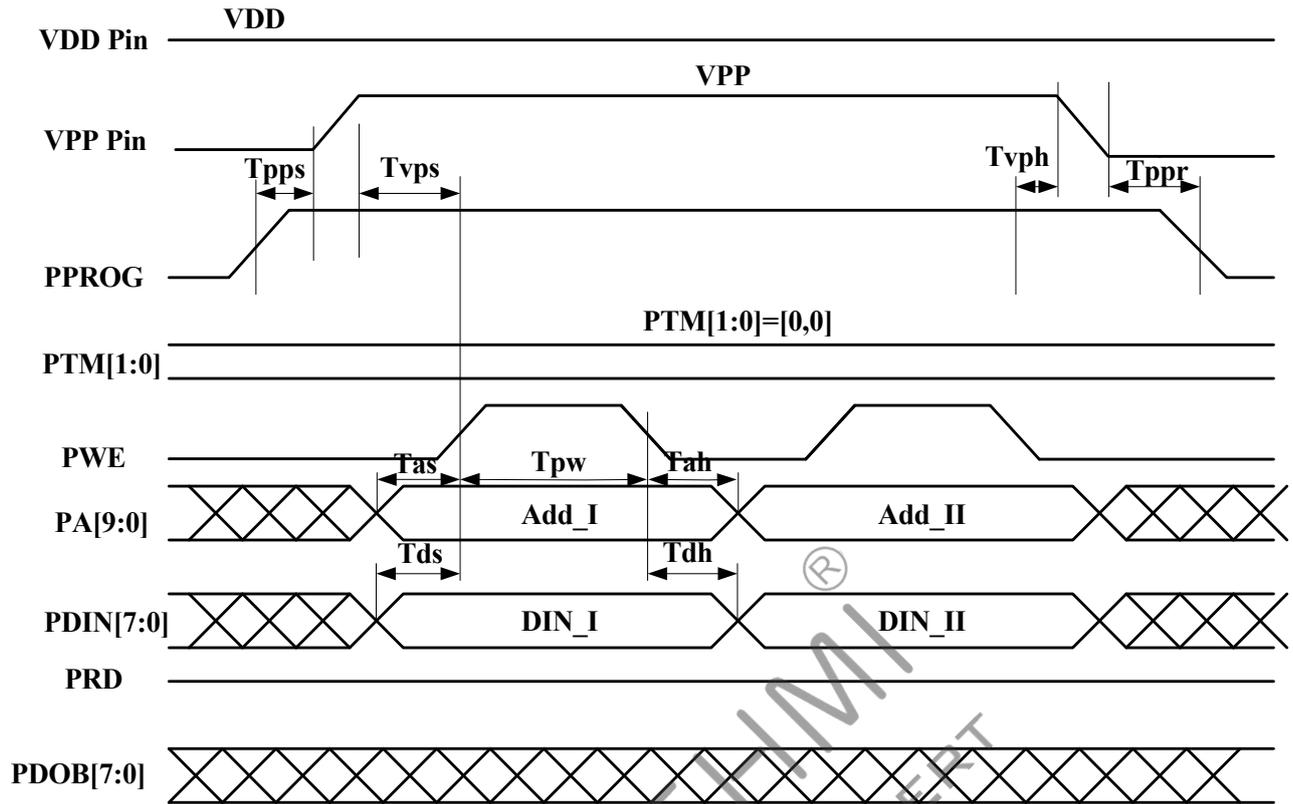
5.12.3 OTP read program flow chart with External Power



When testing, connect signal with the test port, then observe the contend.

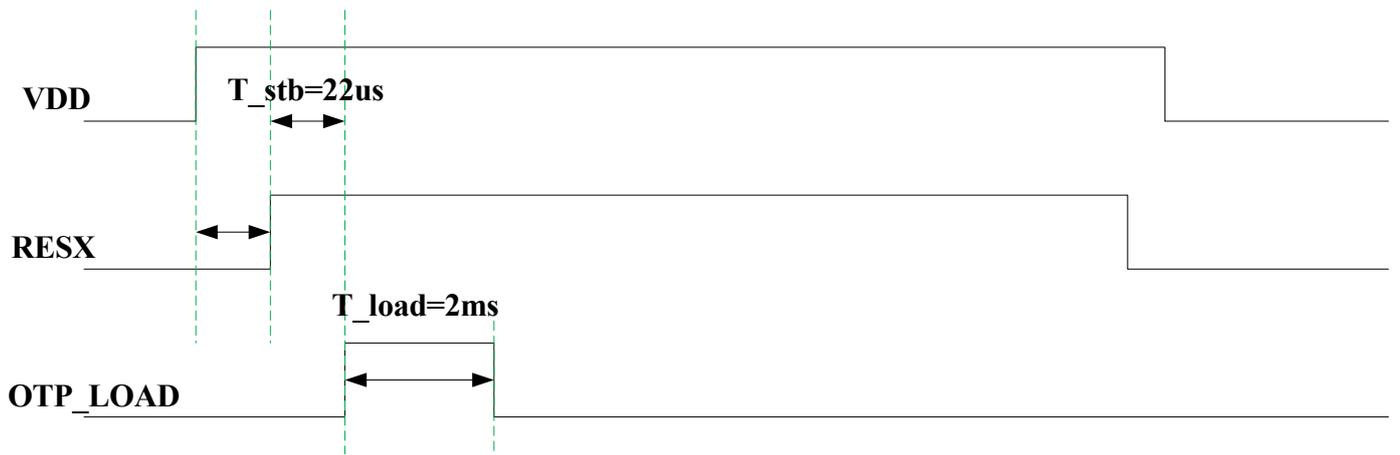
5.12.4 Timing description

Rogram timing :

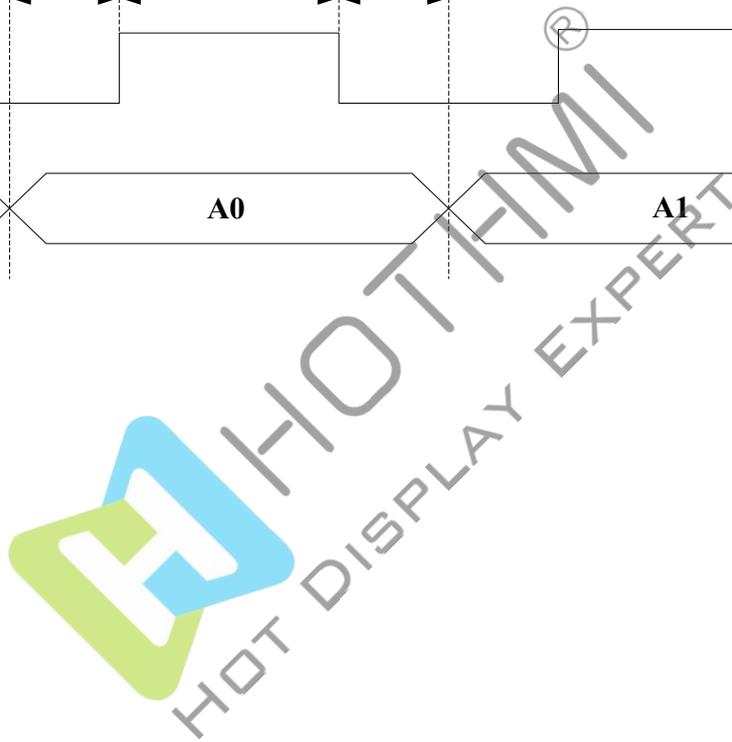
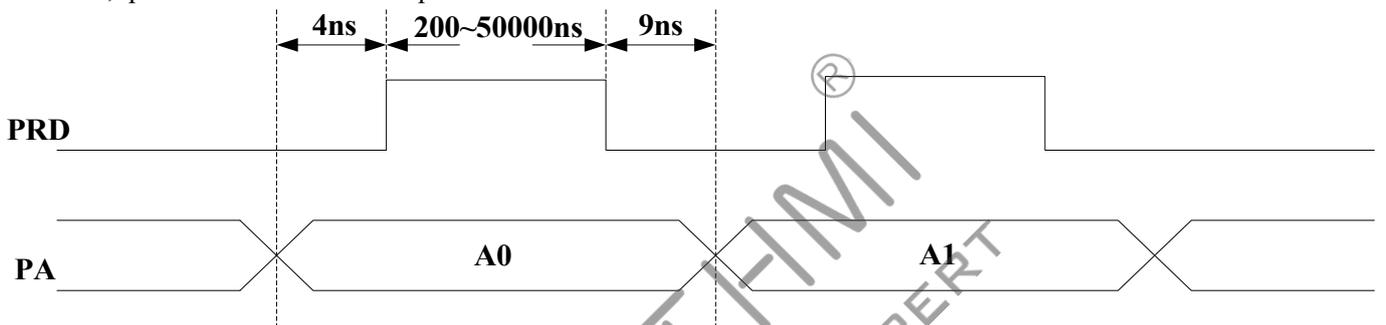


Parameter	Symbol	Min	Max	Unit
Address Setup Time	Tas	4	-	ns
Address Hold Time	Tah	9	-	ns
Data Setup Time	Tds	4	-	ns
Data Hold Time	Tdh	9	-	ns
Program Mode Setup Time	Tpps	10	-	ns
Program Mode Recovery Time	Tppr	10	-	ns
External VPP Setup Time	Tvps	0	-	ns
External VPP Hold Time	Tvph	0	-	ns
Program Pulse Width Time	Tpw	300	350	ns

load otp timing description, time is default value.



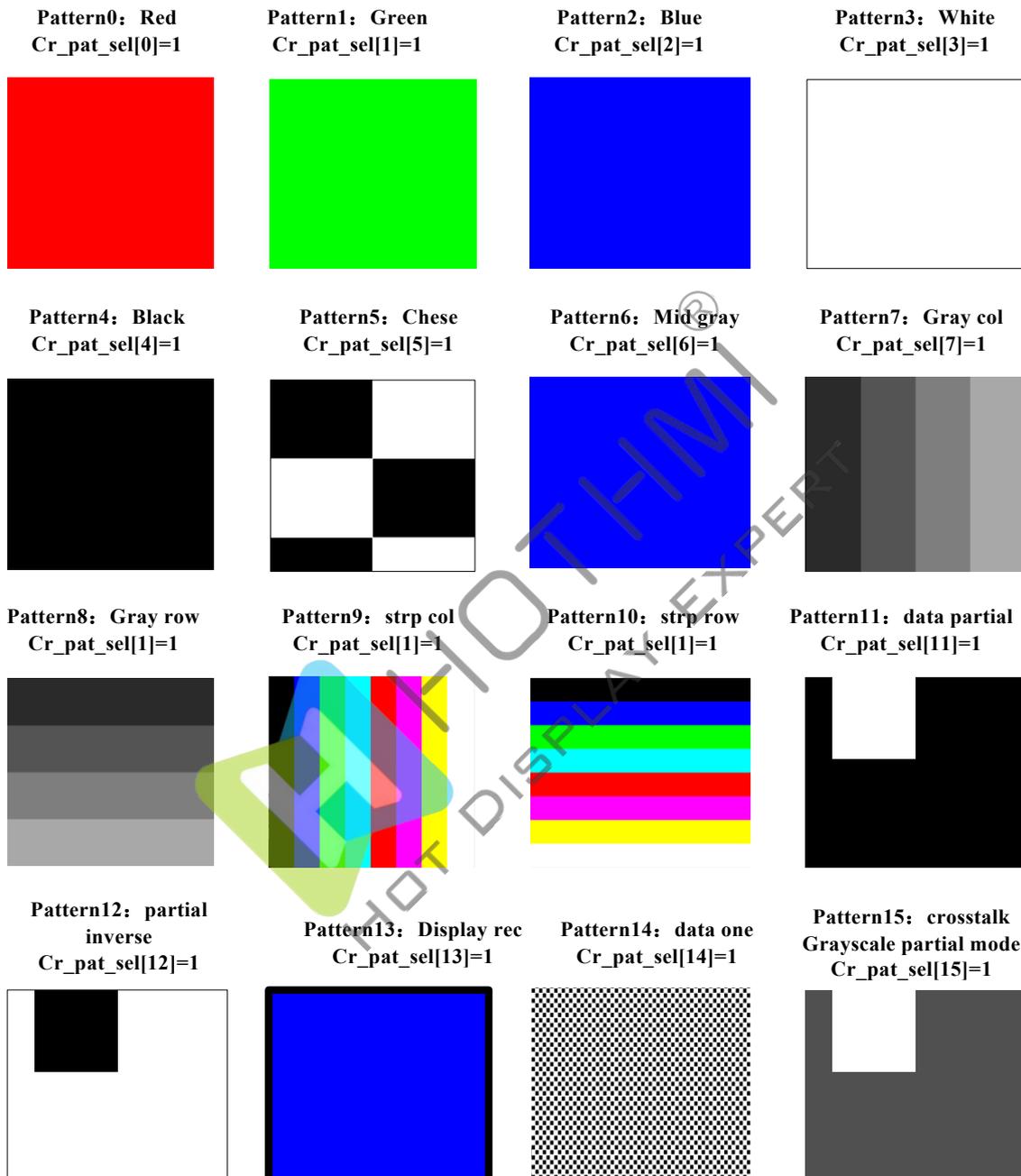
when read, tprd should set as short as possible:



5.13 BIST Function

The BIST (Build In Self Test) is used for inspection, fabrication process and reliability test without external interface operation. this function is controlled by A1 command.

The following BIST patterns are built in the AXS15260D-S1, every pattern and its definition number is also defined as follows:



Note:

- 1.cr_bist_en_mode: Bist mode enable
- 2.cr_pat_sel: display pattern select
- 3.Pattern 6(Mid Gray): RGB value(gray_red,gray_g,gray_b)can be defined by the user;
The default color display blue(gray_red=gray_g=0,gray_b=8'h FF);
- 4.Pattern 13(Display rec):

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RGB value (gray_red,gray_g, gray_b)can be defined by the user;
the default color display blue (gray_red=gray_g=0, gray_b=8'h FF);
but the whole picture will add a black border.

6 ELECTRICAL CHARACTERISTICS

6.1 Absolute Operation Range

VDDI : VDDI VDDI_TP VDDI_F VDDI_LDO VDDI_DRV VDDI_M

Item	Symbol	Min	Max	Unit
Supply Voltage(Analog)	VSP	-0.3	+7.8	V
Supply Voltage(Analog)	VSN	-7.8	+0.3	V
Supply Voltage(I/O)	VDDI	-0.3	+4.0	V
Driver Supply Voltage	VGH-VGL	-0.3	+32	V
Logic Input Voltage Range	VIN	-0.3	VDDI+0.3	V
Logic Output Voltage Range	VO	-0.3	VDDI+0.3	V
Operating Temperature Range	TOPR	-30	+85	°C
Storage Temperature Range	TSTG	-40	+125	°C

6.2

6.2 DC characteristic

6.2.1 Basic DC characteristic

(VSP=4.5V~6.5V, VSN=-6.5V~-4.5V, VDDI = 1.65V~3.6V, Ta = -30°C ~ 70°C)

Parameter	Symbol	Conditions	Specification			Unit	Notes
			MIN	TYP	MAX		
Power & Operation Voltage							
Analog Power	VSP	supply voltage	4.5	5.5	6.5	V	
Analog Power	VSN	supply voltage	-6.5	-5.5	-4.5	V	
Logic Operating voltage (1.8V)	VDDI	supply voltage	-	1.8	-	V	
Logic Operating voltage (3.3V)	VDDI	supply voltage	-	3.3	-	V	
VGH charge pump	VGHOUT1	-	12	15	16	V	
VGH charge pump	VGHOUT2	-	TBD	TBD	TBD	V	
VGL charge pump	VGLOUT1	-	-7.6	-10	-13	V	
VGL charge pump	VGLOUT2	-	TBD	TBD	TBD	V	
VCOM Operation							
VCOM voltage	VCOM	-	-2.5	-	0	V	0
Source Driver							

Source positive output range	Vsout	-	0.5	-	VSP-0.3	V	
Source negative output range	Vsout	-	-0.3	-	VSN+0.3	V	
Reference Voltage							
Internal reference voltage	VREF	-	-	1.8	-	V	
Current Consumption							
Sleep-IN mode(LP-11)	IIOVCC	RESX=High		TBD	TBD	uA	
	IVDD			TBD	TBD	uA	
Sleep-IN mode(ULPS)	IIOVCC	RESX=High		TBD	TBD	uA	
	IVDD			TBD	TBD	uA	

Note:

VGHOUT1:When the external on-load current is below 1.25mA, the maximum voltage can reach 16V, and the register can be adjusted normally;

VGLOUT1:When the external on-load current is below 1.35mA, the minimum voltage can reach -13V, and the register can be adjusted normally.

6.2.2 MIPI DC character

DC characteristics for MIPI-DSI

(VSP=4.5V~6.5V, VSN=-6.5V~-4.5V, VDDI= 1.65V~3.6V, Ta = -30°C ~ 70°C)

Parameter	Symbol	Conditions	Specification			Unit
			MIN	TYP	MAX	
Power supply voltage for MIPI Interface						
Power supply voltage for MIPI interface	VDDI_HS	-		1.8		V
LPDT Input Characteristics						
Pad signal voltage range	VI	-	-50	-	1350	mV
Ground Shift	HS_VSS	-	-50	-	50	mV
Logic 0 input threshold	VIL	-	0	-	550	mV
Logic 1 input threshold	VIH	-	880	-	VDDI_M	mV
Input hysteresis	VHYST	-	25	-	-	mV
LPDT Output Characteristics						
Output low level	VOL	-	-50	-	50	mV
Output high level	VOH	-	1.1	1.2	1.3	V
Logic 1 contention threshold	VIHCD,MIN	-	450	-	HS_LDO	mV
Logic 0 contention threshold	VILCD,MAX	-	0	-	200	mV
Output impedance of LPDT	ZOLP	-	80	-	125	ohm
Hi-speed Input/Output Characteristics						

Single-end input low voltage	VILHS	-	-40	-	-	mV
Single-end input high voltage	VIHHS	-	-	-	460	mV
Common mode voltage	VCMRXDC	-	70	-	330	mV
Hi-speed transmit voltage	VOD	-	140	200	250	mV
Differential input impedance	ZID	-	80	100	125	ohm

6.3 AC characteristic

6.3.1 Reset

The part of touch

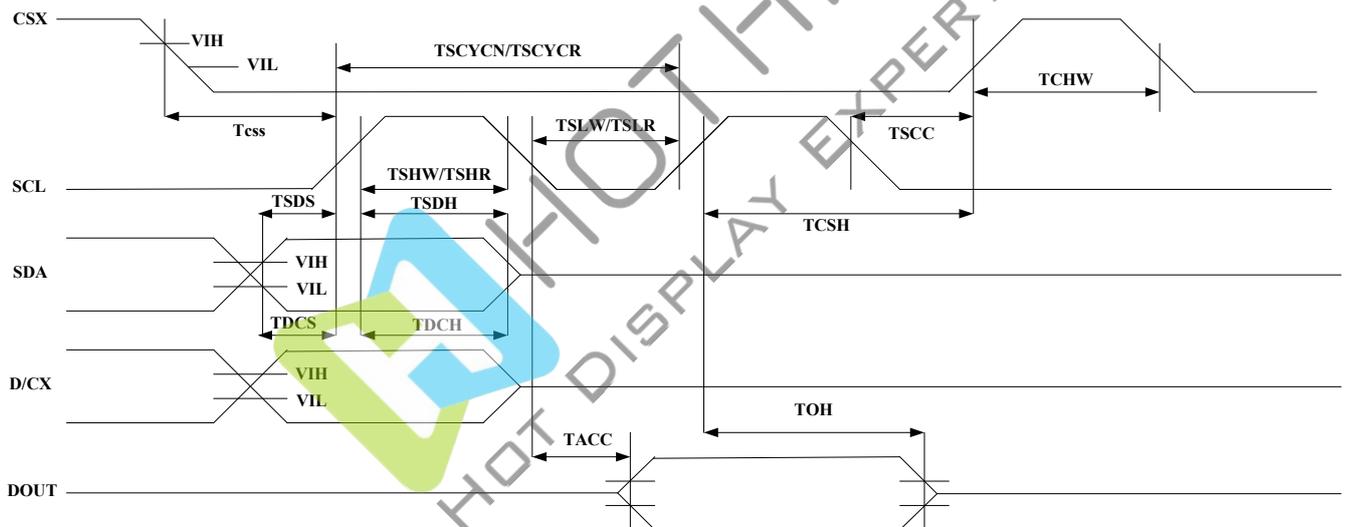
External Reset: 0~VDDI

Soft reset

Host can issue reset instructions to reset the system

6.3.2

6.3.2 Serial interface characteristics (4-line SPI)



Signal	Symbol	Parameter	MIN	MAX	Unit	Description
CSX	T_{CSS}	Chip select setup time (write)	15	-	ns	
	T_{CSH}	Chip select hold time (write)	15	-	ns	
	T_{CSS}	Chip select setup time (read)	60	-	ns	
	T_{SCC}	Chip select hold time (read)	65	-	ns	
	T_{CHW}	Chip select "H" pulse width	40	-	ns	
	T_{SCYCW}	Serial clock cycle (Write)	25	-	ns	-write command & data ram
	T_{SHW}	SCL "H" pulse width (Write)	12	-	ns	
	T_{SLW}	SCL "L" pulse width (Write)	12	-	ns	

SCL	T_{SCYCR}	Serial clock cycle (Read)	25	-	ns	-read command & data ram
	T_{SHR}	SCL “H” pulse width (Read)	12	-	ns	
	T_{SLR}	SCL “L” pulse width (Read)	12	-	ns	
D/CX	T_{DCS}	D/CX setup time	10	-	ns	
	T_{DCH}	D/CX hold time	10	-	ns	
SDA (DIN)	T_{SDS}	Data setup time	10	-	ns	
	T_{SDH}	Data hold time	10	-	ns	
DOUT	T_{ACC}	Access time	10	50	ns	For maximum CL=30pF
	T_{OH}	Output disable time	15	50	ns	For minimum CL=8pF

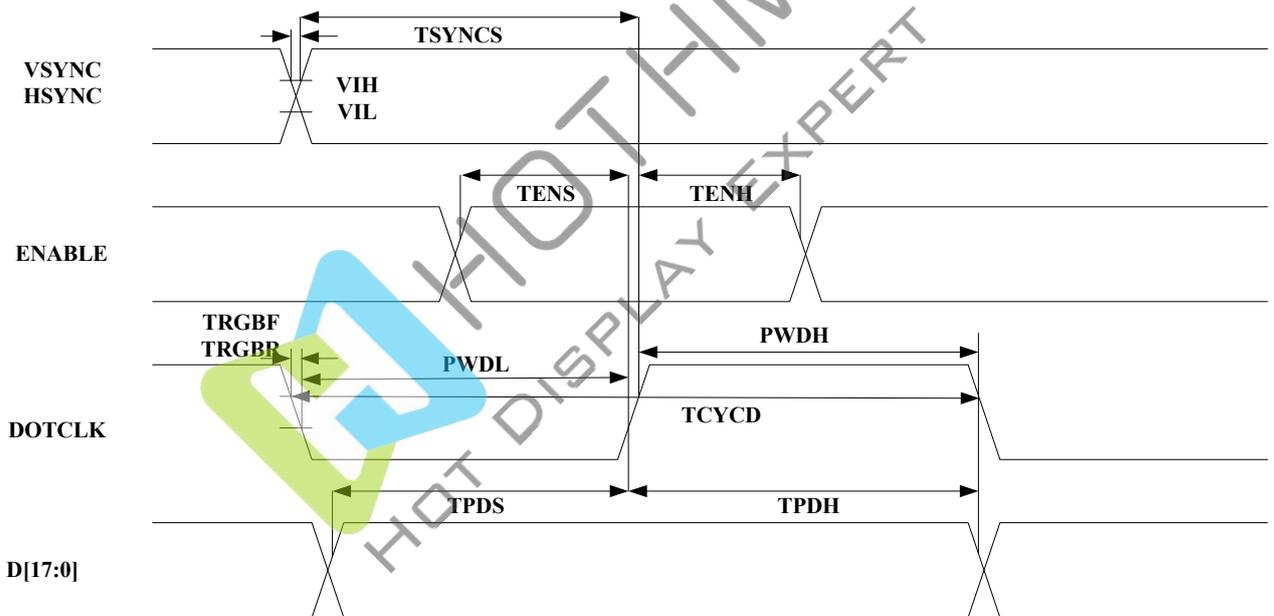
Note 1: VSP=4.5V~6.5V, VSN=-6.5V~-4.5V, VDDI = 1.65V~3.6V, Ta = -30°C ~ 70°C.

Note 2: The input signal rise time and fall time (tr, tf) is specified at 15 ns or less.

Logic high and low levels are specified as 30% and 70% of IOVCC for Input signals.

6.3.3

6.3.3 RGB interface characteristics



RGB Interface Characteristics

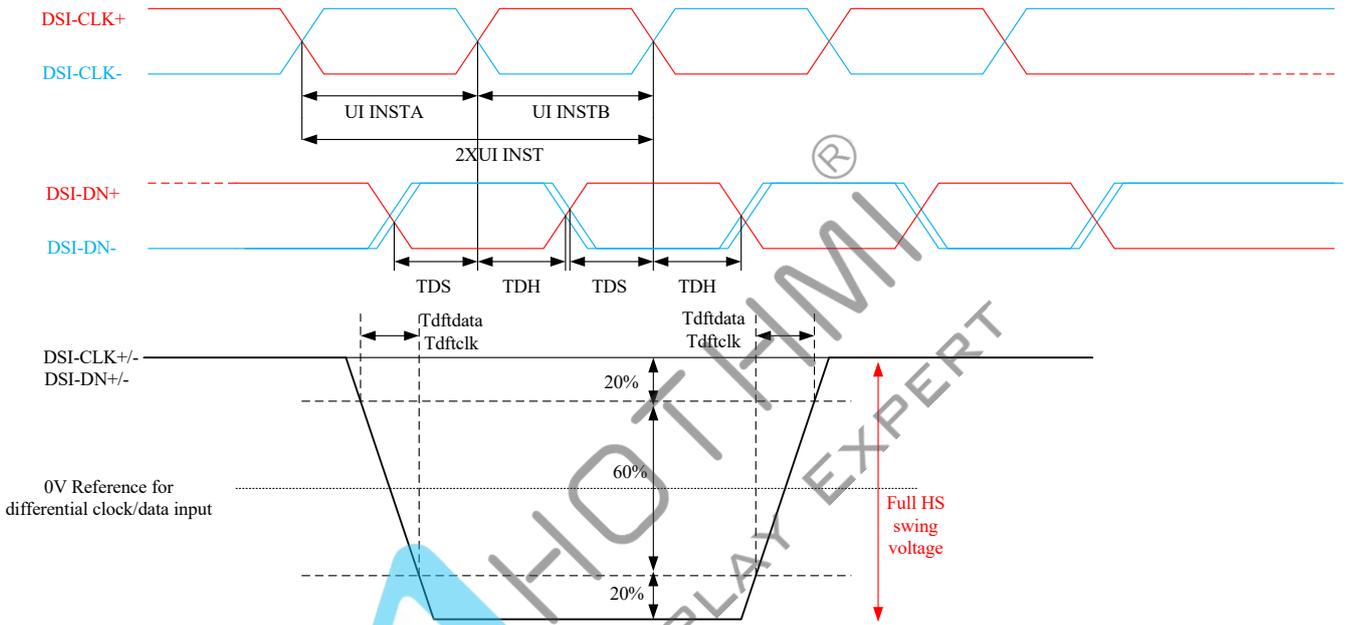
Signal	Symbol	Parameter	Min	Max	Unit	Description
VSYNC/HSYN C	tsyncs	VSYNC/HSYNC setup time	15	-	ns	24/18/16-bit bus RGB
	tsynch	VSYNC/HSYNC hold time	15	-	ns	
DE	tens	DE setup time	15	-	ns	
	tenh	DE hold time	30	-	ns	
D[23:0]	tpds	Data setup time	15	-	ns	
	tpdh	Date hold time	15	-	ns	
	PWDH	DOTCLK high-level period	20	-	ns	

DOTCLK	PWDL	DOTCLK low-level period	20	-	ns	interface mode
	tcy cd	DOTCLK cycle time	40	-	ns	
	trgbr, trgbf	DOTCLK, HSYNC, VSYNC rise/fall time	-	-	ns	

6.3.4

6.3.4 MIPI-DSI characteristics

6.3.4.1 High speed mode



Parameter	Symbol	Parameter	Specification			Unit	Description
			MIN	TYP	MAX		
DSI-CLK+/-	$2xUI_{INSTA}$	Double UI instantaneous	1.6		25	ns	
DSI-CLK+/-	UI_{INSTA} UI_{INSTB}	UI instantaneous halves	0.8		12.5	ns	$UI = UI_{INSTA} = UI_{INSTB}$
DSI-D0+/-	T_{DS}	Data to clock setup time	0.15	-		UI	
DSI-D0+/-	T_{DH}	Data to clock hold time	0.15	-		UI	

Figure: AC characteristics for MIPI-DSI High speed mode

6.3.4.2 Low power mode

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Low Power Mode						

DSI-D0+/-	T_{LPXM}	Length of LP-00, LP-01, LP-10 or LP -11 periods MPU Display Module	50	-	-	ns
DSI-D0+/-	T_{LPXD}	Length of LP-00, LP-01, LP-10 or LP -11 periods Display Module MPU	58	-	-	ns
DSI-D0+/-	$T_{TA-SURED}$	Time-out before the MPU start driving	T LPXD	-	2XT LPXD	ns
DSI-D0+/-	$T_{TA-GETD}$	Time to driver LP-00 by display module	5XT LPXD	-	-	ns
DSI-D0+/-	T_{TA-GOD}	Time to driver LP-00 after turnaround request - MPU	4XT LPXD	-	-	ns
DSI-D0+/-	Ratio T_{LPX}	Ratio of T_{LPXM} / T_{LPXD} between MCU and display module	2/3	-	3/2	

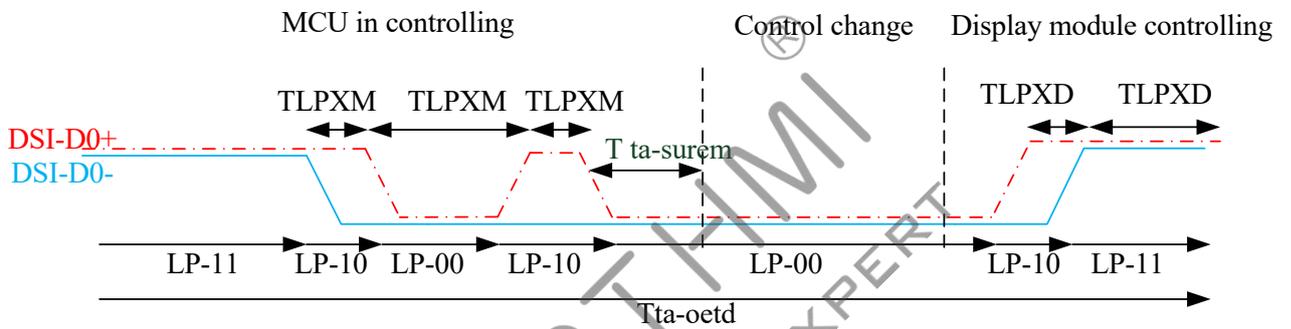


Figure: BTA from the MCU to the Display Module

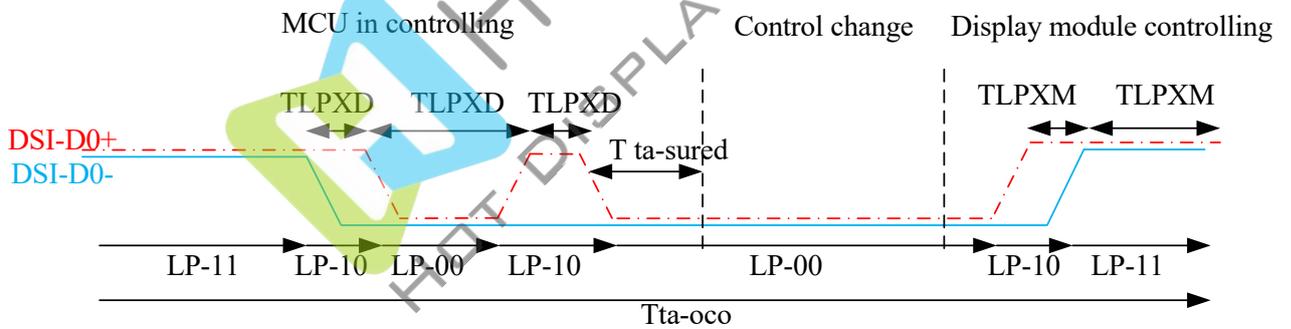


Figure: BTA from the Display Module to the MCU

6.3.4.3 Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
High Speed Data Transmission Bursts						
DSI-Dn+/-	T_{LPX}	Length of any low-power state period	50	-	-	ns
DSI-Dn+/-	$T_{HS-PREPARE}$	Time to driver LP-00 to prepare for HS transmission	40ns + 4UI	-	85ns + 6UI	ns

DSI-Dn+/-	$T_{HS-PREPARE} + T_{HS-ZERO}$	$T_{HS-PREPARE}$ + time to driver HS-0 before the sync sequence	145ns + 10UI	-	-	ns
DSI-Dn+/-	$T_{D-TERM-EN}$	Time to enable Data Lanereceiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	35ns + 4UI	ns
DSI-Dn+/-	$T_{HS-SKIP}$	Time-out at RX to ignore transition period of EoT	40	-	55ns + 4UI	ns
DSI-Dn+/-	$T_{HS-TRAIL}$	Time to driver flipped differential state after last payload data bit of a HS transmission burst	max (8UI, 60ns+4UI)	-	-	ns
DSI-Dn+/-	$T_{HS-EXIT}$	Time to driver LP-11 after HS burst	100	-	-	ns
DSI-Dn+/-	T_{EoT}	Time from start of $T_{HS-TRAIL}$ Period to start of LP-11 state	-	-	105ns + 12UI	ns

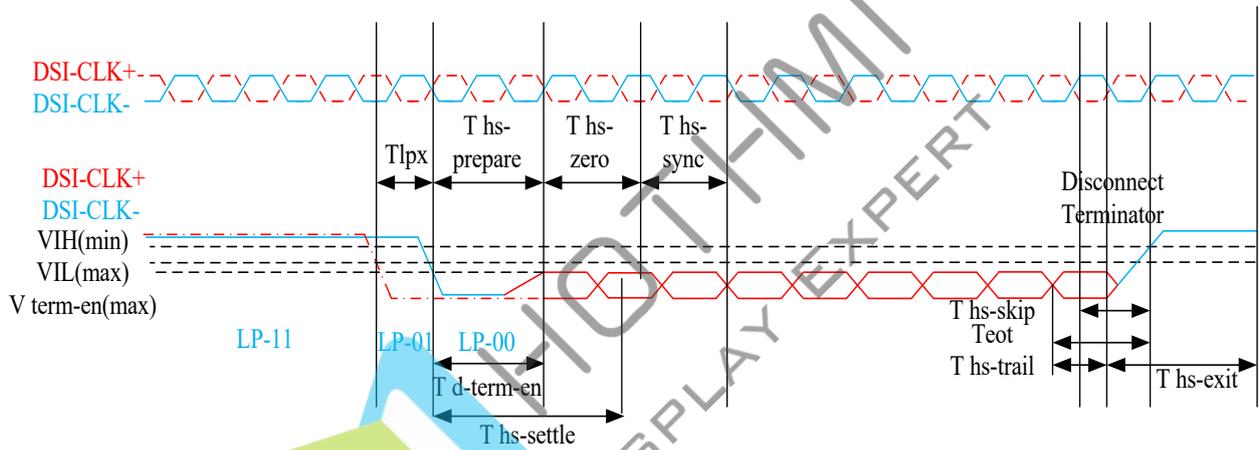


Figure: High Speed Data Transmission Bursts

Parameter	Symbol	Parameter	Specification			Unit
			MIN	TYP	MAX	
Switching the clock Lane between clock Transmission and Low Power Mode						
DSI-CLK+/-	$T_{CLK-POST}$	Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	60ns + 52UI	-	-	ns
DSI-CLK+/-	$T_{CLK-PRE}$	Time that the HS clock shall be driven prior to any associated Data Lane beginning the transition from LP to HS mode	8	-	-	UI
DSI-CLK+/-	$T_{CLK-PREPARE}$	Time to driver LP-00 to prepare for HS clock transmission	38	-	95	ns

DSI-CLK+/-	$T_{CLK-TERM-EN}$	Time to enable Clock Lane receiver line termination measured from when Dn crosses $V_{IL(max)}$	Time for Dn to reach $V_{TERM-EN}$	-	38	ns
DSI-CLK+/-	$T_{CLK-PREPARE} + T_{CLK-ZERO}$	$T_{CLK-PREPARE} +$ time for lead HS-0 driver period before starting Clock	300	-	-	ns
DSI-CLK+/-	$T_{CLK-TRAIL}$	Time to driver HS differential state after last payload clock bit of a HS transmission burst	60	-	-	ns
DSI-CLK+/-	T_{EoT}	Time from start of $T_{CLK-TRAIL}$ period to start of LP-11 state	-	-	105ns + 12UI	ns

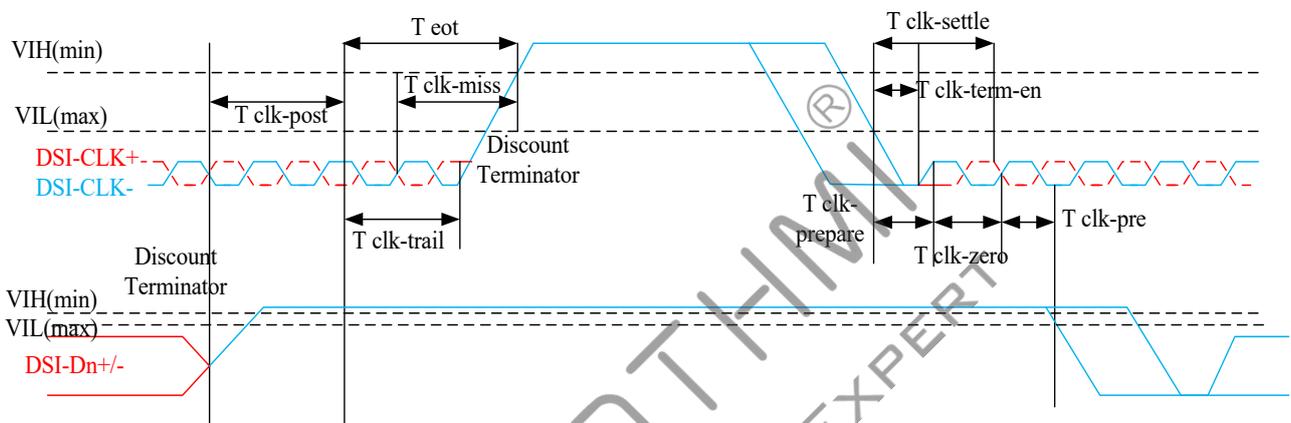


Figure: Switching the clock Lane between clock Transmission and Low Power Mode

6.3.4.4 LP-11 between High Speed and Low Power Modes

DSI-D0 High Speed or Low Power modes are starting or finishing from/to Stop State (SS, LP-11) when

different combinations, what are listed below, are possible:

1. High Speed Mode => Stop State (SS, LP-11) => High Speed Mode
2. High Speed Mode => Stop State (SS, LP-11) => Low Power Mode
3. Low Power Mode => Stop State (SS, LP-11) => High Speed Mode
4. Low Power Mode => Stop State (SS, LP-11) => Low Power Mode

The Low Power Mode is also including 2 different functions:

1. Escape
2. Bus Turnaround (BTA)

Stop State (SS, LP-11) Timings from Previous mode to Next mode

Previous \ Next	Escape mode		HSDT		BTA	
	Min	Max	Min	Max	Min	Max

Escape mode	100ns	-	100ns	-	100ns	-
HSDT	60ns+52UI	-	60ns+52UI	-	60ns+52UI	-
BTA	100ns	-	100ns	-	100ns	-



7 Power Definition

7.1 Start-up time

The part of touch

Power on:

Flash boot $\leq 100\text{ms}$

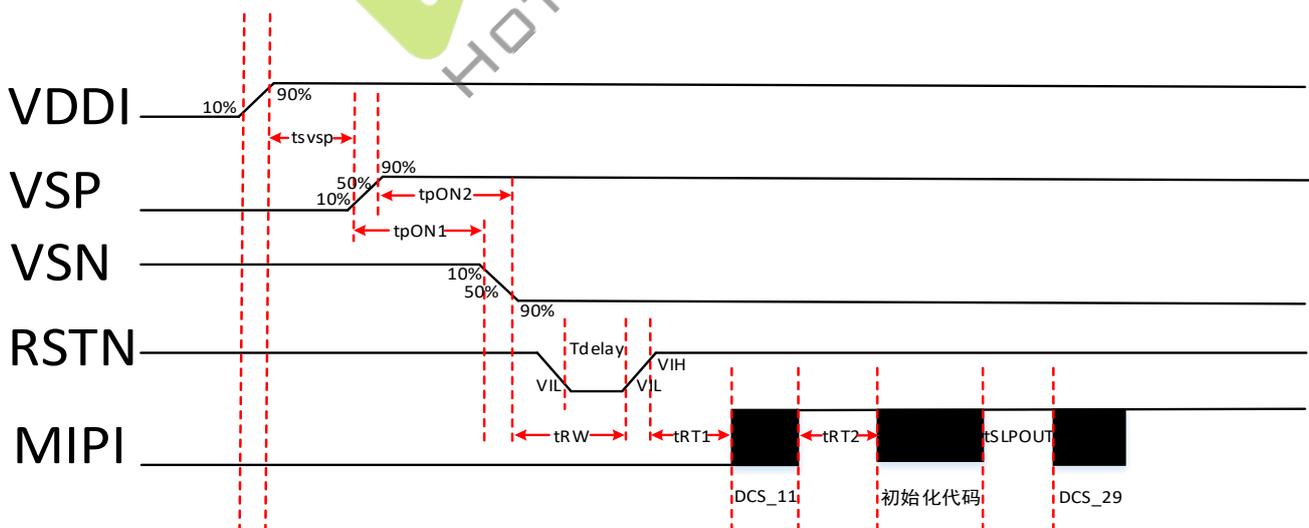
Wake up $\leq 50\text{ms}$

7.2 Power On/Off Sequence

The power on/off sequence is illustrated below:

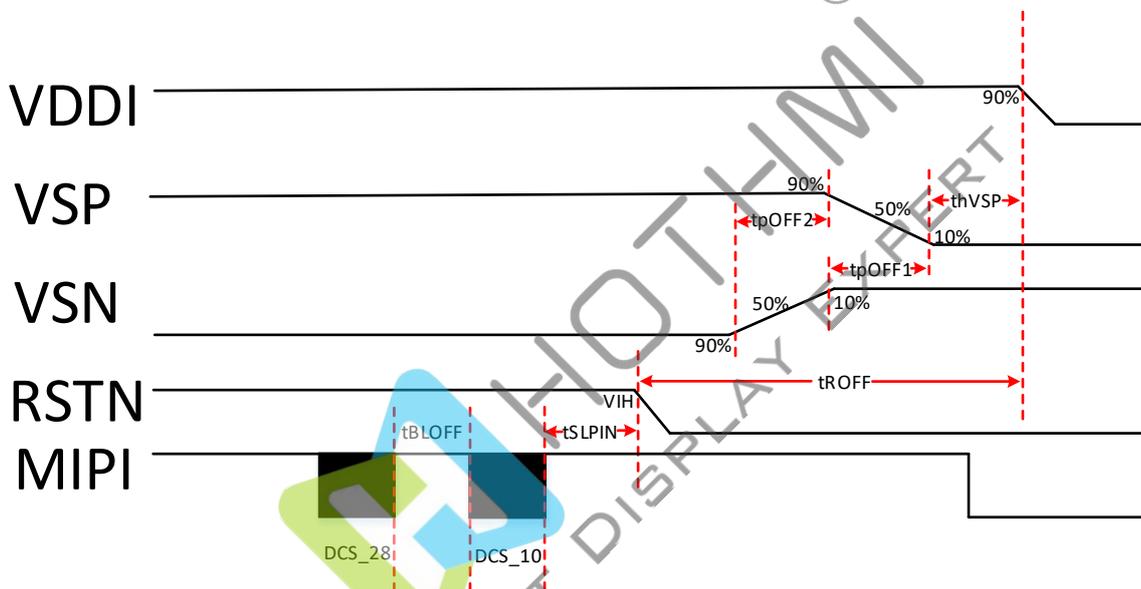
7.2.1 Power on Sequence

Description	Signal	Condition	Typ	Unit
RST Hi-level (VIH) to DCS_11 time	tRT1	Power On	160	ms
SLPOUT Sequence Request time	tSLPOUT	Power On	13.5	ms
VDDI On to VSP On time (90% to 10%)	ts_vsp	Power On	14.7	ms
VSP-VSN delay time (10%-10%)	tPON1	Power On	7.9	ms
VSP-VSN delay time (90%-90%)	tPON2	Power On	8	ms
All Power On to RSTN Hi-level time (90%-VIL)	tRW	Power On	28.7	ms
DCS_11 to 1st Command time	tRT2	Power On	9.9	ms
RSTN delay time	Tdelay	Power On	10	ms



7.2.2 Power off Sequence

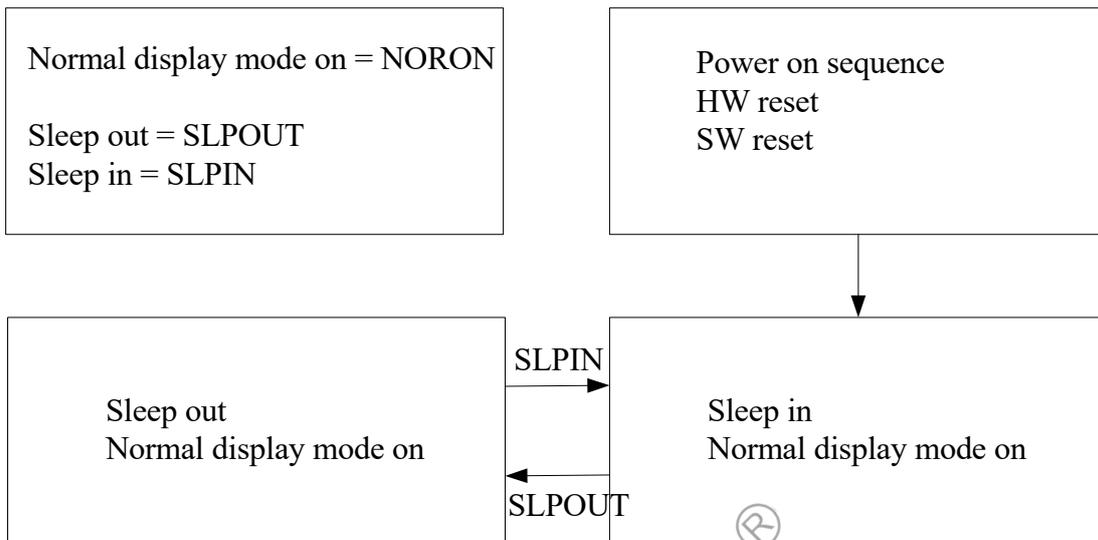
Description	Signal	Condition	Typ	Unit
VSP-VSN delay time (90%-90%)	tPOFF2	Power Off	8.77	ms
VSP-VSN delay time (10%-10%)	tPOFF1	Power Off	3.4	ms
VSP Off to VDDI Off time (10%-90%)	thVSP	Power Off	8.84	ms
RSTN Low to VDDI Off time (VIH to 90%)	tROFF	Power Off	167	ms
SLPIN Sequence Request time	tSLPIN	Power Off	140	ms
DCS_28 to DCS_10 delay time	tBLOFF	Power Off	9.9	ms



7.2.3 Uncontrolled power off

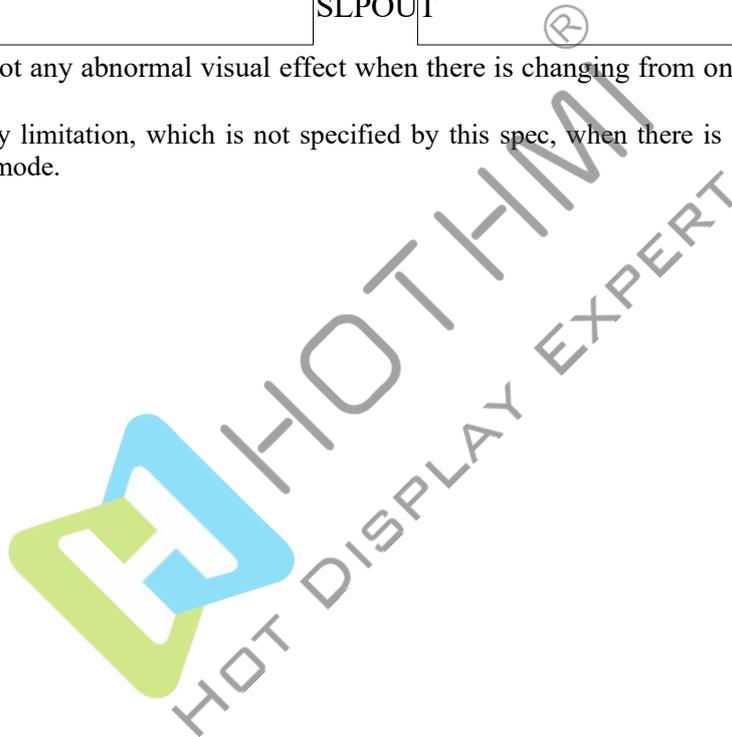
The uncontrolled power off means a situation when e.g. there is removed a battery without the controlled power off sequence. There will not be any damage for the display module or the display module will not cause any damage to the host or lines of the interface. At an uncontrolled power off event, the display will go blank and there will not be any visible effects within (TBD) second on the display (blank display) and remains blank until “Power On Sequence” powers it up.

7.3 Power flow chart

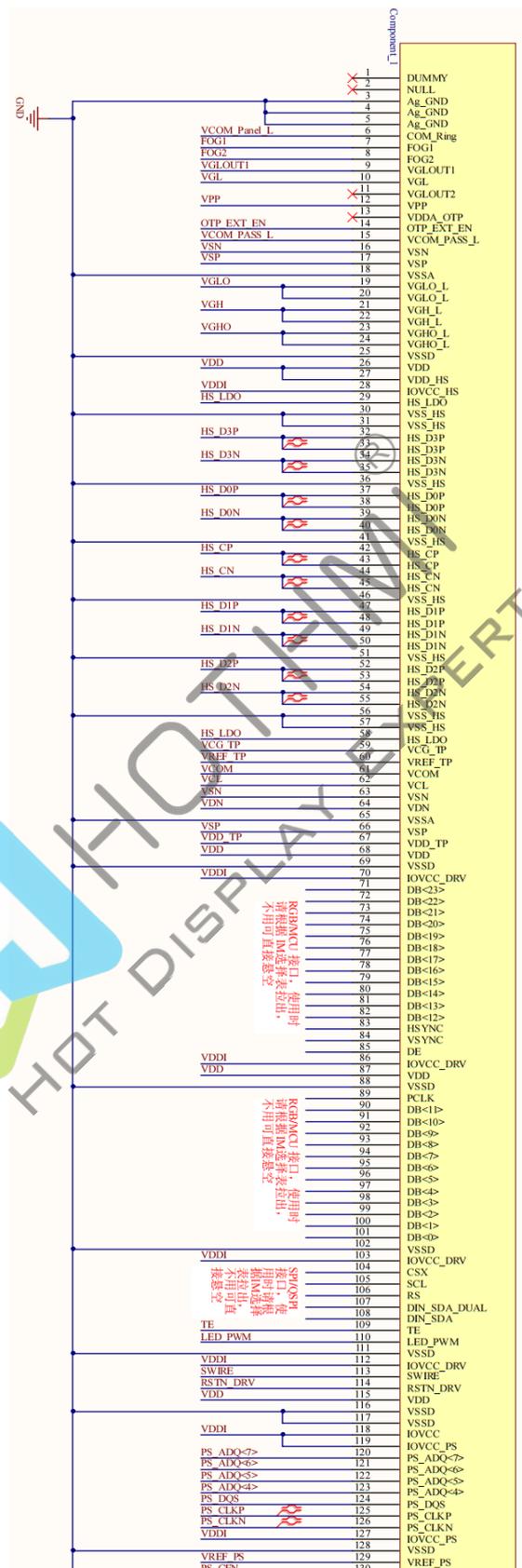


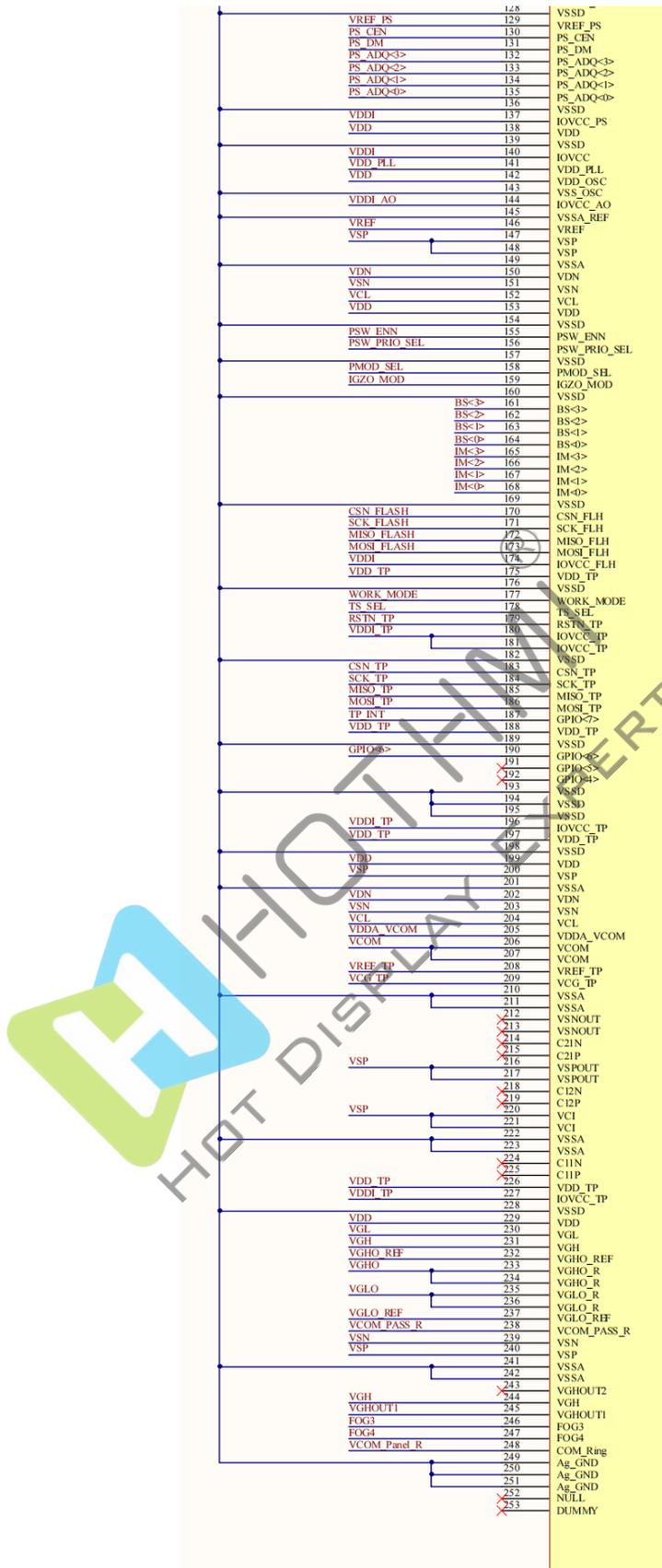
Note 1: There is not any abnormal visual effect when there is changing from one power mode to another power mode.

Note 2: There is not any limitation, which is not specified by this spec, when there is changing from one power mode to another power mode.



8 APPLICATION CIRCUIT





VGHOUT1/2、VGLOUT1/2：panel是a-si工艺用OUT1，LTPS工艺用OUT2

PSW_ENN is power exchanger set pin: 0:enable;1:disable.Default=1

PMOD_SEL is power voltage set pin: 0:when VDDI=3.3v 1:when VDDI=1.8v.Default=1

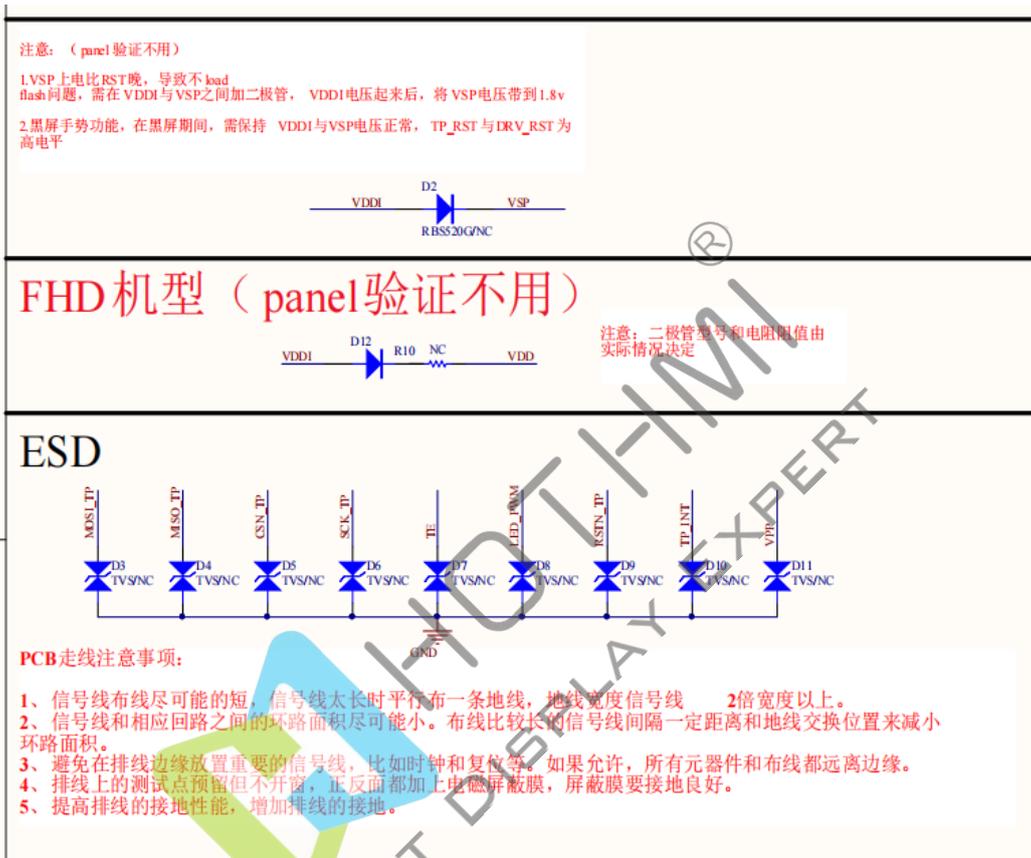
WORK_MODE is Selection of tp work interface : 1:IIC, 0:SPI.Default=0 补充SCK_TP 复用IIC的SCL.MOSI_TP 复用IIC的SDA

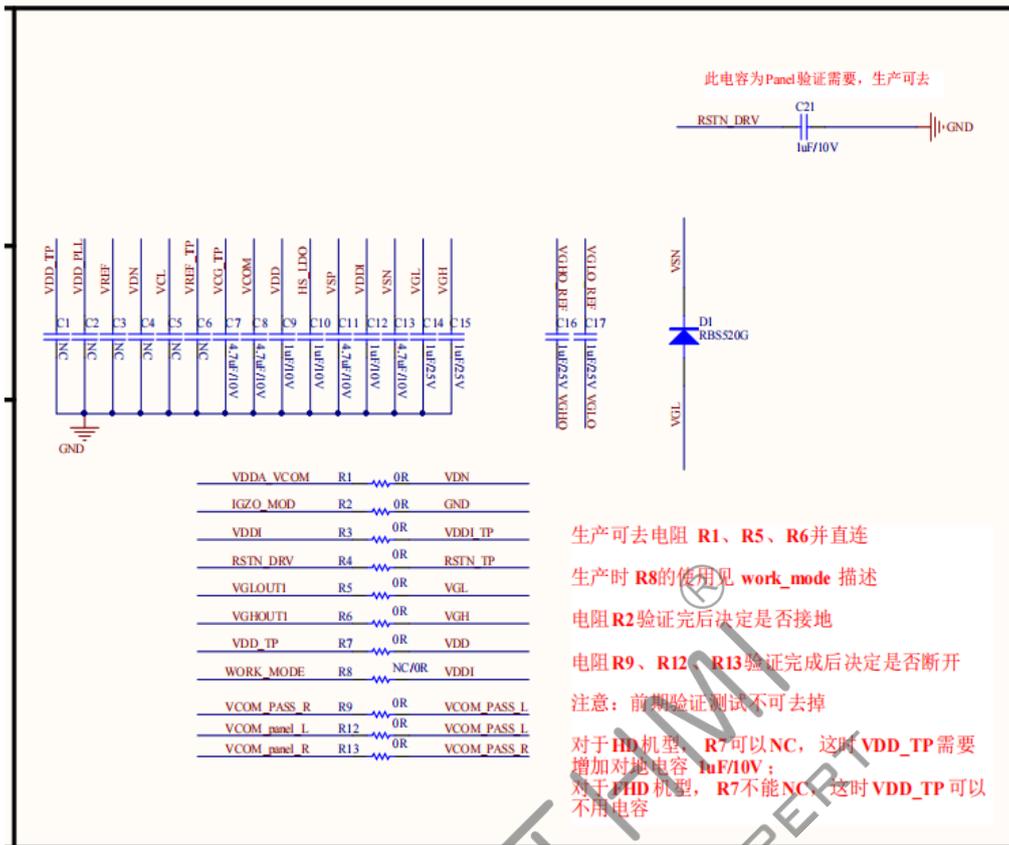
PSW_PRIO_SEL : 0:VDDI_TP 优先, 1:VDDI_DRV 优先.Default=1

TS_SEL : 测试pin

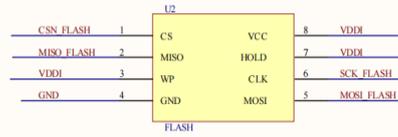
VPP: OTP电源, OTP时需外灌 8.5V

ATEST: 测试pin

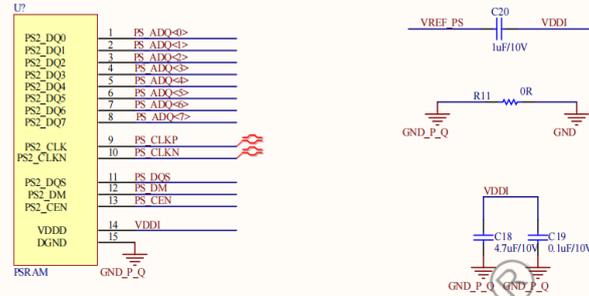




FLASH



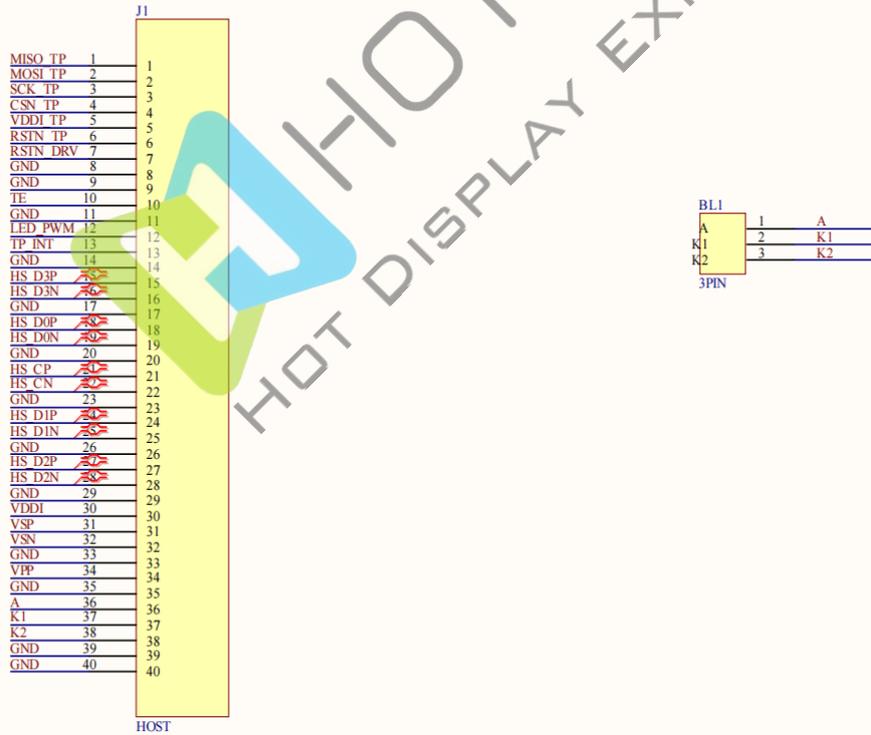
PSRAM (panel验证不用)



- 1.PSRAM 不用时, 所有 pin 可以悬空
- 2.PSRAM 不用时, 需要关掉使能 (使能默认关)
- 3.psr.am 数据线尽量短, 等长, 间隔不要太近

接口

背光



IM<3>	R14	0R/NC	GND
IM<2>	R15	0R/NC	GND
IM<1>	R16	0R/NC	GND
IM<0>	R17	0R/NC	GND

使用时请根据IM选择表拉出，内置上拉电阻，选1时可直接悬空，选0接GND

BS<3>	R18	0R/NC	GND
BS<2>	R19	0R/NC	GND
BS<1>	R20	0R/NC	GND
BS<0>	R21	0R/NC	GND

使用时请根据BS选择表拉出，内置上拉电阻，选1时可直接悬空，选0接GND

涉及15260版本兼容，请优先选择左侧表格的红色字体顺序

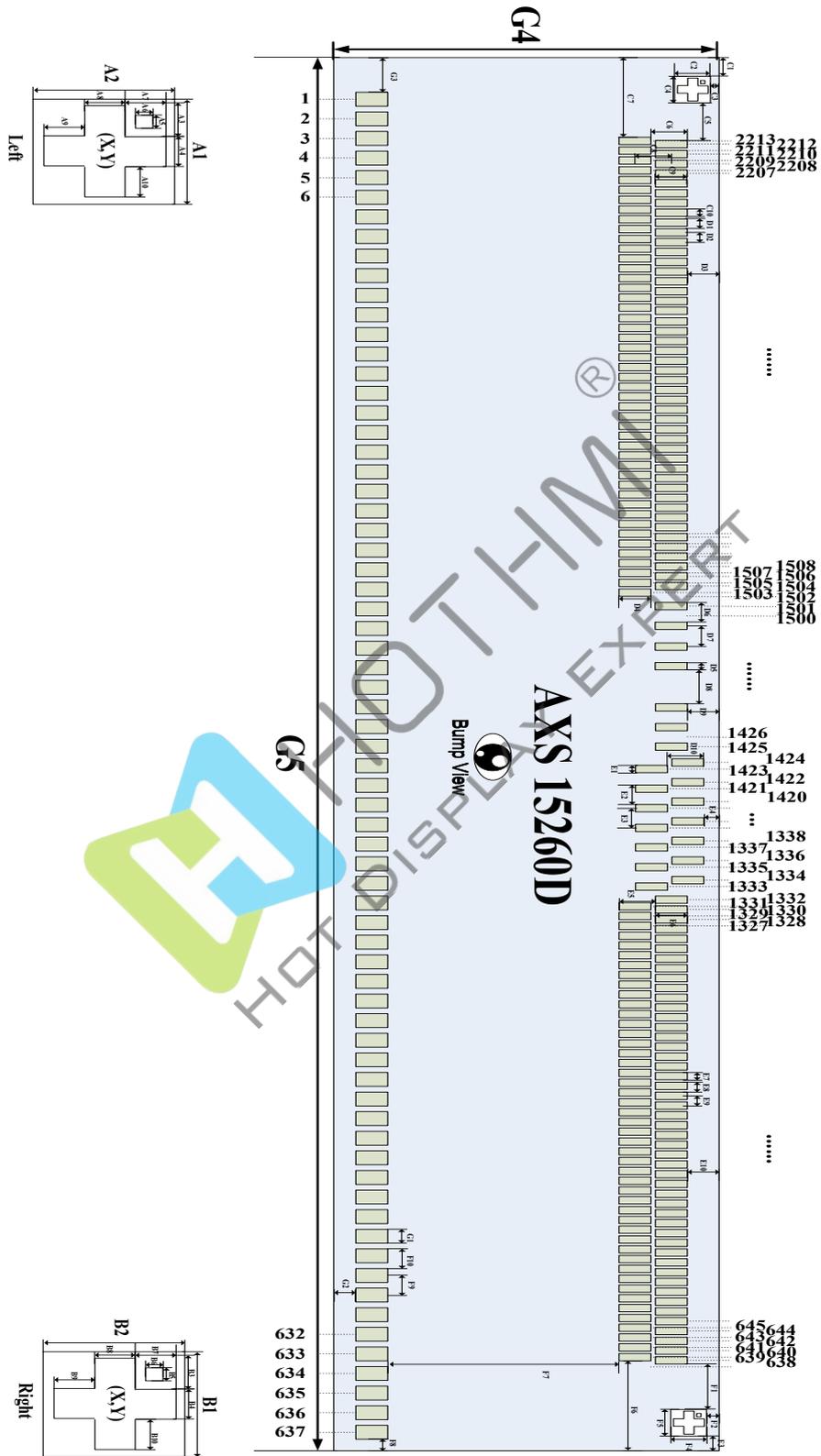
BS<3>: 0>内置上拉电阻，不需外部上拉

Note : pls contact AXS if you have any question.



9 CHIP INFORMATION

9.1 PAD Assignment



Symb ol	Size	Symb ol	Size	Symb ol	Size	Symb ol	Size	Symb ol	Size
A1	80	A2	80	A3	15	A4	20	A5	10
A6	10	A7	15	A8	20	A9	15	A10	15
B1	80	B2	80	B3	15	B4	20	B5	10
B6	10	B7	15	B8	20	B9	15	B10	15
C1	50	C2	80	C3	50	C4	80	C5	264/262
C6	100	C7	382/380	C8	100	C9	75	C10	12
D1	24/23.99	D2	24/23.99	D3	81.28	D4	75	D5	12
D6	47.98/47.99/48	D7	47.98/47.99/48	D8	335.92/336	D9	81.28	D10	100
E1	12	E2	71.99/71.98/72	E3	71.99/71.98/72	E4	35.28	E5	100
E6	75	E7	12	E8	24/23.99	E9	24/23.99	E10	81.28
F1	252/250	F2	50	F3	50	F4	80	F5	80
F6	394/392	F7	441.22	F8	88.76/86	F9	38.99/39	F10	38.99/39
G1	24	G2	47.5	G3	88.76/86	G4	820	G5	25000
									Unit=um

Item	PAD No.	Size		Unit
		X	Y	
Chip Size	-	25000	820	um
Chip thickness	-	200		
Pad Size	1 - 637	24	75	
	638 - 1332	12	75	
	1333 - 1424	12	75	
	1425 - 1463	12	75	
	1464 - 1502	12	75	
	1503 - 2213	12	75	
Pad Pitch	1 - 637	38.99/39	-	
	638 - 1332	11.99/12	100	
	1333 - 1424	11.99/12	100	
	1425 - 1463	47.98/47.99/48	-	
	1464 - 1502	47.98/47.99/48	-	
	1503 - 2213	11.99/12	100	

Note1: Have Temperature compensation design.

9.2 PAD CENTER COORDINATE

PAD NO	PAD name	X	Y	PAD NO	PAD name	X	Y
1	VGLOUT1	-12399.24	-325	1108	VSSA	6472.56	291.22
2	VGLOUT1	-12360.25	-325	1109	VSSA	6460.56	191.22
3	VGL	-12321.26	-325	1110	VSSA	6448.57	291.223
4	VGL	-12282.27	-325	1111	VSSA	6436.57	191.22
5	VGLOUT2	-12243.28	-325	1112	VSSA	6424.57	291.22
6	VGLOUT2	-12204.29	-325	1113	SX<320>	6412.57	191.22
7	VPP	-12165.3	-325	1114	S<540>	6400.58	291.22
8	VPP	-12126.3	-325	1115	S<539>	6388.58	191.22
9	VDDA_OTP	-12087.31	-325	1116	VSSA	6376.58	291.22
10	VDDA_OTP	-12048.32	-325	1117	S<538>	6364.59	191.22
11	OTP_EXT_EN	-12009.33	-325	1118	SX<319>	6352.59	291.22
12	VCOM_PASS_L	-11970.34	-325	1119	S<537>	6340.59	191.22
13	VSN	-11931.35	-325	1120	S<536>	6328.59	291.22
14	VSN	-11892.36	-325	1121	VSSA	6316.6	191.22
15	VSP	-11853.37	-325	1122	S<535>	6304.6	291.22
16	VSP	-11814.37	-325	1123	SX<318>	6292.6	191.22
17	VSSA	-11775.38	-325	1124	S<534>	6280.6	291.22
18	VSSA	-11736.39	-325	1125	S<533>	6268.61	191.22
19	VSSA	-11697.4	-325	1126	VSSA	6256.61	291.22
20	VGLO_L	-11658.41	-325	1127	S<532>	6244.61	191.22
21	VGLO_L	-11619.42	-325	1128	SX<317>	6232.61	291.22
22	VGLO_L	-11580.43	-325	1129	S<531>	6220.62	191.22
23	VGLO_L	-11541.43	-325	1130	S<530>	6208.62	291.22
24	VGLO_L	-11502.44	-325	1131	VSSA	6196.62	191.22
25	VGH_L	-11463.45	-325	1132	S<529>	6184.63	291.22
26	VGH_L	-11424.46	-325	1133	SX<316>	6172.63	191.22
27	VGH_L	-11385.47	-325	1134	S<528>	6160.63	291.22
28	VGH_L	-11346.48	-325	1135	S<527>	6148.63	191.22
29	VGH_L	-11307.49	-325	1136	SX<315>	6136.64	291.22
30	VGHO_L	-11268.5	-325	1137	S<526>	6124.64	191.22
31	VGHO_L	-11229.5	-325	1138	SX<314>	6112.64	291.22
32	VGHO_L	-11190.51	-325	1139	S<525>	6100.64	191.22
33	VGHO_L	-11151.52	-325	1140	S<524>	6088.65	291.22
34	VGHO_L	-11112.53	-325	1141	SX<313>	6076.65	191.22
35	CGOUT_L<1>	-11073.54	-325	1142	S<523>	6064.65	291.22
36	CGOUT_L<2>	-11034.55	-325	1143	SX<312>	6052.65	191.22
37	CGOUT_L<3>	-10995.56	-325	1144	S<522>	6040.66	291.22
38	CGOUT_L<4>	-10956.56	-325	1145	S<521>	6028.66	191.22
39	CGOUT_L<5>	-10917.57	-325	1146	SX<311>	6016.66	291.22
40	CGOUT_L<6>	-10878.58	-325	1147	S<520>	6004.67	191.22
41	CGOUT_L<7>	-10839.59	-325	1148	SX<310>	5992.67	291.22
42	CGOUT_L<8>	-10800.6	-325	1149	S<519>	5980.67	191.22
43	CGOUT_L<9>	-10761.61	-325	1150	S<518>	5968.67	291.22

44	CGOUT_L<10>	-10722.62	-325	1151	SX<309>	5956.68	191.22
45	CGOUT_L<11>	-10683.63	-325	1152	S<517>	5944.68	291.22
46	CGOUT_L<12>	-10644.63	-325	1153	SX<308>	5932.68	191.22
47	CGOUT_L<13>	-10605.64	-325	1154	S<516>	5920.68	291.22
48	CGOUT_L<14>	-10566.65	-325	1155	S<515>	5908.69	191.22
49	CGOUT_L<15>	-10527.66	-325	1156	SX<307>	5896.69	291.22
50	CGOUT_L<16>	-10488.67	-325	1157	S<514>	5884.69	191.22
51	CGOUT_L<17>	-10449.68	-325	1158	SX<306>	5872.69	291.22
52	VSSD	-10410.69	-325	1159	S<513>	5860.7	191.22
53	VSSD	-10371.69	-325	1160	S<512>	5848.7	291.22
54	VSSD	-10332.7	-325	1161	SX<305>	5836.7	191.22
55	VDD	-10293.71	-325	1162	S<511>	5824.71	291.22
56	VDD	-10254.72	-325	1163	SX<304>	5812.71	191.22
57	VDD	-10215.73	-325	1164	S<510>	5800.71	291.22
58	VDD_HS	-10176.74	-325	1165	S<509>	5788.71	191.22
59	VDD_HS	-10137.75	-325	1166	SX<303>	5776.72	291.22
60	VDD_HS	-10098.76	-325	1167	S<508>	5764.72	191.22
61	VDD_HS	-10059.76	-325	1168	SX<302>	5752.72	291.22
62	VDDI_HS	-10020.77	-325	1169	S<507>	5740.72	191.22
63	VDDI_HS	-9981.78	-325	1170	S<506>	5728.73	291.22
64	VDDI_HS	-9942.79	-325	1171	SX<301>	5716.73	191.22
65	VDDI_HS	-9903.8	-325	1172	S<505>	5704.73	291.22
66	HS_LDO	-9864.81	-325	1173	SX<300>	5692.73	191.22
67	HS_LDO	-9825.82	-325	1174	S<504>	5680.74	291.22
68	HS_LDO	-9786.82	-325	1175	S<503>	5668.74	191.22
69	HS_LDO	-9747.83	-325	1176	SX<299>	5656.74	291.22
70	VSS_HS	-9708.84	-325	1177	S<502>	5644.75	191.22
71	VSS_HS	-9669.85	-325	1178	SX<298>	5632.75	291.22
72	VSS_HS	-9630.86	-325	1179	S<501>	5620.75	191.22
73	VSS_HS	-9591.87	-325	1180	S<500>	5608.75	291.22
74	HS_D3P	-9552.88	-325	1181	SX<297>	5596.76	191.22
75	HS_D3P	-9513.89	-325	1182	S<499>	5584.76	291.22
76	HS_D3P	-9474.89	-325	1183	SX<296>	5572.76	191.22
77	HS_D3P	-9435.9	-325	1184	S<498>	5560.76	291.22
78	HS_D3N	-9396.91	-325	1185	S<497>	5548.77	191.22
79	HS_D3N	-9357.92	-325	1186	SX<295>	5536.77	291.22
80	HS_D3N	-9318.93	-325	1187	S<496>	5524.77	191.22
81	HS_D3N	-9279.94	-325	1188	SX<294>	5512.77	291.22
82	VSS_HS	-9240.95	-325	1189	S<495>	5500.78	191.22
83	VSS_HS	-9201.95	-325	1190	S<494>	5488.78	291.22
84	HS_D0P	-9162.96	-325	1191	SX<293>	5476.78	191.22
85	HS_D0P	-9123.97	-325	1192	S<493>	5464.79	291.22
86	HS_D0P	-9084.98	-325	1193	SX<292>	5452.79	191.22
87	HS_D0P	-9045.99	-325	1194	S<492>	5440.79	291.22
88	HS_D0N	-9007	-325	1195	S<491>	5428.79	191.22
89	HS_D0N	-8968.01	-325	1196	SX<291>	5416.8	291.22
90	HS_D0N	-8929.02	-325	1197	S<490>	5404.8	191.22

91	HS_D0N	-8890.02	-325	1198	SX<290>	5392.8	291.22
92	VSS_HS	-8851.03	-325	1199	S<489>	5380.8	191.22
93	VSS_HS	-8812.04	-325	1200	S<488>	5368.81	291.22
94	HS_CP	-8773.05	-325	1201	SX<289>	5356.81	191.22
95	HS_CP	-8734.06	-325	1202	S<487>	5344.81	291.22
96	HS_CP	-8695.07	-325	1203	SX<288>	5332.81	191.22
97	HS_CP	-8656.08	-325	1204	S<486>	5320.82	291.22
98	HS_CN	-8617.08	-325	1205	S<485>	5308.82	191.22
99	HS_CN	-8578.09	-325	1206	VSSA	5296.82	291.22
100	HS_CN	-8539.1	-325	1207	S<484>	5284.83	191.22
101	HS_CN	-8500.11	-325	1208	SX<287>	5272.83	291.22
102	VSS_HS	-8461.12	-325	1209	S<483>	5260.83	191.22
103	VSS_HS	-8422.13	-325	1210	S<482>	5248.83	291.22
104	HS_D1P	-8383.14	-325	1211	VSSA	5236.84	191.22
105	HS_D1P	-8344.15	-325	1212	S<481>	5224.84	291.22
106	HS_D1P	-8305.15	-325	1213	SX<286>	5212.84	191.22
107	HS_D1P	-8266.16	-325	1214	S<480>	5200.84	291.22
108	HS_D1N	-8227.17	-325	1215	S<479>	5188.85	191.22
109	HS_D1N	-8188.18	-325	1216	VSSA	5176.85	291.22
110	HS_D1N	-8149.19	-325	1217	S<478>	5164.85	191.22
111	HS_D1N	-8110.2	-325	1218	SX<285>	5152.85	291.22
112	VSS_HS	-8071.21	-325	1219	S<477>	5140.86	191.22
113	VSS_HS	-8032.21	-325	1220	S<476>	5128.86	291.22
114	HS_D2P	-7993.22	-325	1221	VSSA	5116.86	191.22
115	HS_D2P	-7954.23	-325	1222	S<475>	5104.87	291.22
116	HS_D2P	-7915.24	-325	1223	SX<284>	5092.87	191.22
117	HS_D2P	-7876.25	-325	1224	S<474>	5080.87	291.22
118	HS_D2N	-7837.26	-325	1225	S<473>	5068.87	191.22
119	HS_D2N	-7798.27	-325	1226	SX<283>	5056.88	291.22
120	HS_D2N	-7759.28	-325	1227	S<472>	5044.88	191.22
121	HS_D2N	-7720.28	-325	1228	SX<282>	5032.88	291.22
122	VSS_HS	-7681.29	-325	1229	S<471>	5020.88	191.22
123	VSS_HS	-7642.3	-325	1230	S<470>	5008.89	291.22
124	VSS_HS	-7603.31	-325	1231	SX<281>	4996.89	191.22
125	VSS_HS	-7564.32	-325	1232	S<469>	4984.89	291.22
126	HS_LDO	-7525.33	-325	1233	SX<280>	4972.89	191.22
127	HS_LDO	-7486.34	-325	1234	S<468>	4960.9	291.22
128	HS_LDO	-7447.34	-325	1235	S<467>	4948.9	191.22
129	HS_LDO	-7408.35	-325	1236	SX<279>	4936.9	291.22
130	VCG_TP	-7369.36	-325	1237	S<466>	4924.91	191.22
131	VCG_TP	-7330.37	-325	1238	SX<278>	4912.91	291.22
132	VREF_TP	-7291.38	-325	1239	S<465>	4900.91	191.22
133	VREF_TP	-7252.39	-325	1240	S<464>	4888.91	291.22
134	VCOM	-7213.4	-325	1241	SX<277>	4876.92	191.22
135	VCOM	-7174.41	-325	1242	S<463>	4864.92	291.22
136	ATEST0_NV	-7135.41	-325	1243	SX<276>	4852.92	191.22
137	VCL	-7096.42	-325	1244	S<462>	4840.92	291.22

138	VCL	-7057.43	-325	1245	S<461>	4828.93	191.22
139	VSN	-7018.44	-325	1246	SX<275>	4816.93	291.22
140	VSN	-6979.45	-325	1247	S<460>	4804.93	191.22
141	VSN	-6940.46	-325	1248	SX<274>	4792.93	291.22
142	VDN	-6901.47	-325	1249	S<459>	4780.94	191.22
143	VDN	-6862.47	-325	1250	S<458>	4768.94	291.22
144	VDN	-6823.48	-325	1251	SX<273>	4756.94	191.22
145	VSSA	-6784.49	-325	1252	S<457>	4744.95	291.22
146	VSSA	-6745.5	-325	1253	SX<272>	4732.95	191.22
147	VSSA	-6706.51	-325	1254	S<456>	4720.95	291.22
148	VSP	-6667.52	-325	1255	S<455>	4708.95	191.22
149	VSP	-6628.53	-325	1256	SX<271>	4696.96	291.22
150	VSP	-6589.54	-325	1257	S<454>	4684.96	191.22
151	ATEST1_PV	-6550.54	-325	1258	SX<270>	4672.96	291.22
152	ATEST2_LV	-6511.55	-325	1259	S<453>	4660.96	191.22
153	VDD_TP	-6472.56	-325	1260	S<452>	4648.97	291.22
154	VDD_TP	-6433.57	-325	1261	SX<269>	4636.97	191.22
155	VDD	-6394.58	-325	1262	S<451>	4624.97	291.22
156	VDD	-6355.59	-325	1263	SX<268>	4612.97	191.22
157	VDD	-6316.6	-325	1264	S<450>	4600.98	291.22
158	VDD	-6277.6	-325	1265	S<449>	4588.98	191.22
159	VSSD	-6238.61	-325	1266	SX<267>	4576.98	291.22
160	VSSD	-6199.62	-325	1267	S<448>	4564.99	191.22
161	VSSD	-6160.63	-325	1268	SX<266>	4552.99	291.22
162	VSSD	-6121.64	-325	1269	S<447>	4540.99	191.22
163	VDDI_DRV	-6082.65	-325	1270	S<446>	4528.99	291.22
164	VDDI_DRV	-6043.66	-325	1271	SX<265>	4517	191.22
165	DB<23>	-6004.67	-325	1272	S<445>	4505	291.22
166	DB<23>	-5965.67	-325	1273	SX<264>	4493	191.22
167	DB<22>	-5926.68	-325	1274	S<444>	4481	291.22
168	DB<22>	-5887.69	-325	1275	S<443>	4469.01	191.22
169	DB<21>	-5848.7	-325	1276	SX<263>	4457.01	291.22
170	DB<21>	-5809.71	-325	1277	S<442>	4445.01	191.22
171	DB<20>	-5770.72	-325	1278	SX<262>	4433.01	291.22
172	DB<20>	-5731.73	-325	1279	S<441>	4421.02	191.22
173	DB<19>	-5692.73	-325	1280	S<440>	4409.02	291.22
174	DB<19>	-5653.74	-325	1281	SX<261>	4397.02	191.22
175	DB<18>	-5614.75	-325	1282	S<439>	4385.03	291.22
176	DB<18>	-5575.76	-325	1283	SX<260>	4373.03	191.22
177	DB<17>	-5536.77	-325	1284	S<438>	4361.03	291.22
178	DB<17>	-5497.78	-325	1285	S<437>	4349.03	191.22
179	DB<16>	-5458.79	-325	1286	SX<259>	4337.04	291.22
180	DB<16>	-5419.8	-325	1287	S<436>	4325.04	191.22
181	DB<15>	-5380.8	-325	1288	SX<258>	4313.04	291.22
182	DB<15>	-5341.81	-325	1289	S<435>	4301.04	191.22
183	DB<14>	-5302.82	-325	1290	S<434>	4289.05	291.22
184	DB<14>	-5263.83	-325	1291	SX<257>	4277.05	191.22

185	DB<13>	-5224.84	-325	1292	S<433>	4265.05	291.22
186	DB<13>	-5185.85	-325	1293	SX<256>	4253.05	191.22
187	DB<12>	-5146.86	-325	1294	S<432>	4241.06	291.22
188	DB<12>	-5107.86	-325	1295	S<431>	4229.06	191.22
189	HSYNC	-5068.87	-325	1296	SX<255>	4217.06	291.22
190	HSYNC	-5029.88	-325	1297	S<430>	4205.07	191.22
191	VSYNC	-4990.89	-325	1298	SX<254>	4193.07	291.22
192	VSYNC	-4951.9	-325	1299	S<429>	4181.07	191.22
193	DE	-4912.91	-325	1300	S<428>	4169.07	291.22
194	DE	-4873.92	-325	1301	SX<253>	4157.08	191.22
195	VDDI_DRV	-4834.93	-325	1302	S<427>	4145.08	291.22
196	VDDI_DRV	-4795.93	-325	1303	SX<252>	4133.08	191.22
197	VDD	-4756.94	-325	1304	S<426>	4121.08	291.22
198	VDD	-4717.95	-325	1305	S<425>	4109.09	191.22
199	VSSD	-4678.96	-325	1306	SX<251>	4097.09	291.22
200	VSSD	-4639.97	-325	1307	S<424>	4085.09	191.22
201	PCLK	-4600.98	-325	1308	SX<250>	4073.09	291.22
202	PCLK	-4561.99	-325	1309	S<423>	4061.1	191.22
203	DB<11>	-4522.99	-325	1310	S<422>	4049.1	291.22
204	DB<11>	-4484	-325	1311	SX<249>	4037.1	191.22
205	DB<10>	-4445.01	-325	1312	S<421>	4025.11	291.22
206	DB<10>	-4406.02	-325	1313	SX<248>	4013.11	191.22
207	DB<9>	-4367.03	-325	1314	S<420>	4001.11	291.22
208	DB<9>	-4328.04	-325	1315	S<419>	3989.11	191.22
209	DB<8>	-4289.05	-325	1316	SX<247>	3977.12	291.22
210	DB<8>	-4250.06	-325	1317	S<418>	3965.12	191.22
211	DB<7>	-4211.06	-325	1318	SX<246>	3953.12	291.22
212	DB<7>	-4172.07	-325	1319	S<417>	3941.12	191.22
213	DB<6>	-4133.08	-325	1320	S<416>	3929.13	291.22
214	DB<6>	-4094.09	-325	1321	SX<245>	3917.13	191.22
215	DB<5>	-4055.1	-325	1322	S<415>	3905.13	291.22
216	DB<5>	-4016.11	-325	1323	SX<244>	3893.13	191.22
217	DB<4>	-3977.12	-325	1324	S<414>	3881.14	291.22
218	DB<4>	-3938.12	-325	1325	S<413>	3869.14	191.22
219	DB<3>	-3899.13	-325	1326	SX<243>	3857.14	291.22
220	DB<3>	-3860.14	-325	1327	S<412>	3845.15	191.22
221	DB<2>	-3821.15	-325	1328	SX<242>	3833.15	291.22
222	DB<2>	-3782.16	-325	1329	S<411>	3821.15	191.22
223	DB<1>	-3743.17	-325	1330	S<410>	3809.15	291.22
224	DB<1>	-3704.18	-325	1331	SX<241>	3797.16	191.22
225	DB<0>	-3665.19	-325	1332	S<409>	3785.16	291.22
226	DB<0>	-3626.19	-325	1333	DUMMY	3725.17	237.22
227	VSSD	-3587.2	-325	1334	DUMMY	3713.17	337.22
228	VSSD	-3548.21	-325	1335	DUMMY	3653.19	237.22
229	VDDI_DRV	-3509.22	-325	1336	DUMMY	3641.19	337.22
230	VDDI_DRV	-3470.23	-325	1337	DUMMY	3581.2	237.22
231	CSX	-3431.24	-325	1338	DUMMY	3569.21	337.22

232	CSX	-3392.25	-325	1339	DUMMY	3509.22	237.22
233	SCL	-3353.25	-325	1340	DUMMY	3497.22	337.22
234	SCL	-3314.26	-325	1341	DUMMY	3437.24	237.22
235	RS	-3275.27	-325	1342	DUMMY	3425.24	337.22
236	RS	-3236.28	-325	1343	DUMMY	3365.25	237.22
237	DIN_SDA_DUAL	-3197.29	-325	1344	DUMMY	3353.25	337.22
238	DIN_SDA_DUAL	-3158.3	-325	1345	DUMMY	3293.27	237.22
239	DIN_SDA	-3119.31	-325	1346	DUMMY	3281.27	337.22
240	DIN_SDA	-3080.32	-325	1347	DUMMY	3221.28	237.22
241	TE	-3041.32	-325	1348	DUMMY	3209.29	337.22
242	TE	-3002.33	-325	1349	DUMMY	3149.3	237.22
243	LED_PWM	-2963.34	-325	1350	DUMMY	3137.3	337.22
244	LED_PWM	-2924.35	-325	1351	DUMMY	3077.32	237.22
245	VSSD	-2885.36	-325	1352	DUMMY	3065.32	337.22
246	VSSD	-2846.37	-325	1353	DUMMY	3005.33	237.22
247	VDDI_DRV	-2807.38	-325	1354	DUMMY	2993.33	337.22
248	VDDI_DRV	-2768.38	-325	1355	DUMMY	2933.35	237.22
249	SWIRE	-2729.39	-325	1356	DUMMY	2921.35	337.22
250	SWIRE	-2690.4	-325	1357	DUMMY	2861.36	237.22
251	RSTN_DRV	-2651.41	-325	1358	DUMMY	2849.37	337.22
252	RSTN_DRV	-2612.42	-325	1359	DUMMY	2789.38	237.22
253	VDD	-2573.43	-325	1360	DUMMY	2777.38	337.22
254	VDD	-2534.44	-325	1361	DUMMY	2717.4	237.22
255	VDD	-2495.45	-325	1362	DUMMY	2705.4	337.22
256	VDD	-2456.45	-325	1363	DUMMY	2645.41	237.22
257	VSSD	-2417.46	-325	1364	DUMMY	2633.41	337.22
258	VSSD	-2378.47	-325	1365	DUMMY	2573.43	237.22
259	VSSD	-2339.48	-325	1366	DUMMY	2561.43	337.22
260	VSSD	-2300.49	-325	1367	DUMMY	2501.44	237.22
261	VSSD	-2261.5	-325	1368	DUMMY	2489.45	337.22
262	VDDI	-2222.51	-325	1369	DUMMY	2429.46	237.22
263	VDDI	-2183.51	-325	1370	DUMMY	2417.46	337.22
264	VDDI	-2144.52	-325	1371	DUMMY	2357.48	237.22
265	VDDI	-2105.53	-325	1372	DUMMY	2345.48	337.22
266	ATEST3_LV	-2066.54	-325	1373	DUMMY	2285.49	237.22
267	VDDI_PS	-2027.55	-325	1374	DUMMY	2273.49	337.22
268	VDDI_PS	-1988.56	-325	1375	DUMMY	2213.51	237.22
269	VDDI_PS	-1949.57	-325	1376	DUMMY	2201.51	337.22
270	VDDI_PS	-1910.58	-325	1377	DUMMY	2141.52	237.22
271	PS_ADQ<7>	-1871.58	-325	1378	DUMMY	2129.53	337.22
272	PS_ADQ<7>	-1832.59	-325	1379	DUMMY	2069.54	237.22
273	PS_ADQ<6>	-1793.6	-325	1380	DUMMY	2057.54	337.22
274	PS_ADQ<6>	-1754.61	-325	1381	DUMMY	1997.56	237.22
275	PS_ADQ<5>	-1715.62	-325	1382	DUMMY	1985.56	337.22
276	PS_ADQ<5>	-1676.63	-325	1383	DUMMY	1925.57	237.22
277	PS_ADQ<4>	-1637.64	-325	1384	DUMMY	1913.57	337.22
278	PS_ADQ<4>	-1598.64	-325	1385	DUMMY	1853.59	237.22

279	PS_DQS	-1559.65	-325	1386	DUMMY	1841.59	337.22
280	PS_DQS	-1520.66	-325	1387	DUMMY	1781.6	237.22
281	PS_CLKP	-1481.67	-325	1388	DUMMY	1769.61	337.22
282	PS_CLKP	-1442.68	-325	1389	DUMMY	1709.62	237.22
283	PS_CLKN	-1403.69	-325	1390	DUMMY	1697.62	337.22
284	PS_CLKN	-1364.7	-325	1391	DUMMY	1637.64	237.22
285	VDDI_PS	-1325.71	-325	1392	DUMMY	1625.64	337.22
286	VDDI_PS	-1286.71	-325	1393	DUMMY	1565.65	237.22
287	VDDI_PS	-1247.72	-325	1394	DUMMY	1553.65	337.22
288	VDDI_PS	-1208.73	-325	1395	DUMMY	1493.67	237.22
289	VSSD	-1169.74	-325	1396	DUMMY	1481.67	337.22
290	VSSD	-1130.75	-325	1397	DUMMY	1421.68	237.22
291	VSSD	-1091.76	-325	1398	DUMMY	1409.69	337.22
292	VSSD	-1052.77	-325	1399	DUMMY	1349.7	237.22
293	VREF_PS	-1013.77	-325	1400	DUMMY	1337.7	337.22
294	VREF_PS	-974.78	-325	1401	DUMMY	1277.72	237.22
295	VREF_PS	-935.79	-325	1402	DUMMY	1265.72	337.22
296	VREF_PS	-896.8	-325	1403	DUMMY	1205.73	237.22
297	PS_CEN	-857.81	-325	1404	DUMMY	1193.73	337.22
298	PS_CEN	-818.82	-325	1405	DUMMY	1133.75	237.22
299	PS_DM	-779.83	-325	1406	DUMMY	1121.75	337.22
300	PS_DM	-740.84	-325	1407	DUMMY	1061.76	237.22
301	PS_ADQ<3>	-701.84	-325	1408	DUMMY	1049.77	337.22
302	PS_ADQ<3>	-662.85	-325	1409	DUMMY	989.78	237.22
303	PS_ADQ<2>	-623.86	-325	1410	DUMMY	977.78	337.22
304	PS_ADQ<2>	-584.87	-325	1411	DUMMY	917.8	237.22
305	PS_ADQ<1>	-545.88	-325	1412	DUMMY	905.8	337.22
306	PS_ADQ<1>	-506.89	-325	1413	DUMMY	845.81	237.22
307	PS_ADQ<0>	-467.9	-325	1414	DUMMY	833.81	337.22
308	PS_ADQ<0>	-428.9	-325	1415	DUMMY	773.83	237.22
309	VSSD	-389.91	-325	1416	DUMMY	761.83	337.22
310	VSSD	-350.92	-325	1417	DUMMY	701.84	237.22
311	VSSD	-311.93	-325	1418	DUMMY	689.85	337.22
312	VSSD	-272.94	-325	1419	DUMMY	629.86	237.22
313	VDDI_PS	-233.95	-325	1420	DUMMY	617.86	337.22
314	VDDI_PS	-194.96	-325	1421	DUMMY	557.88	237.22
315	VDDI_PS	-155.97	-325	1422	DUMMY	545.88	337.22
316	VDDI_PS	-116.97	-325	1423	DUMMY	485.89	237.22
317	VDD	-77.98	-325	1424	DUMMY	473.89	337.22
318	VDD	-38.99	-325	1425	DUMMY	437.9	291.22
319	VSSD	0	-325	1426	DUMMY	389.91	291.22
320	VSSD	38.99	-325	1427	DUMMY	341.92	291.22
321	VSSD	77.98	-325	1428	DUMMY	293.93	291.22
322	VDDI	116.97	-325	1429	DUMMY	245.95	291.22
323	VDDI	155.97	-325	1430	DUMMY	197.96	291.22
324	VDDI	194.96	-325	1431	DUMMY	149.97	291.22
325	VDDI	233.95	-325	1432	DUMMY	101.98	291.22

326	VDD_PLL	272.94	-325	1433	DUMMY	53.99	291.22
327	VDD_PLL	311.93	-325	1434	DUMMY	6	291.22
328	VDD_OSC	350.92	-325	1435	DUMMY	-41.99	291.22
329	VDD_OSC	389.91	-325	1436	DUMMY	-89.98	291.22
330	VSS_OSC	428.9	-325	1437	DUMMY	-137.97	291.22
331	VSS_OSC	467.9	-325	1438	DUMMY	-185.96	291.22
332	OSC_IN	506.89	-325	1439	DUMMY	-233.95	291.22
333	OSC_TE	545.88	-325	1440	DUMMY	-281.94	291.22
334	VDDI_AO	584.87	-325	1441	DUMMY	-329.93	291.22
335	VDDI_AO	623.86	-325	1442	DUMMY	-377.92	291.22
336	VSSA_REF	662.85	-325	1443	DUMMY	-425.91	291.22
337	VSSA_REF	701.84	-325	1444	DUMMY	-473.89	291.22
338	VREF	740.84	-325	1445	DUMMY	-521.88	291.22
339	VREF	779.83	-325	1446	DUMMY	-569.87	291.22
340	VREF	818.82	-325	1447	DUMMY	-617.86	291.22
341	ATEST5_PV	857.81	-325	1448	DUMMY	-665.85	291.22
342	VSP	896.8	-325	1449	DUMMY	-713.84	291.22
343	VSP	935.79	-325	1450	DUMMY	-761.83	291.22
344	VSP	974.78	-325	1451	DUMMY	-809.82	291.22
345	VSP	1013.77	-325	1452	DUMMY	-857.81	291.22
346	VSP	1052.77	-325	1453	DUMMY	-905.8	291.22
347	VSSA	1091.76	-325	1454	DUMMY	-953.79	291.22
348	VSSA	1130.75	-325	1455	DUMMY	-1001.78	291.22
349	VSSA	1169.74	-325	1456	DUMMY	-1049.77	291.22
350	VSSA	1208.73	-325	1457	DUMMY	-1097.76	291.22
351	VDN	1247.72	-325	1458	DUMMY	-1145.75	291.22
352	VDN	1286.71	-325	1459	DUMMY	-1193.73	291.22
353	VDN	1325.71	-325	1460	DUMMY	-1241.72	291.22
354	VDN	1364.7	-325	1461	DUMMY	-1289.71	291.22
355	VSN	1403.69	-325	1462	DUMMY	-1337.7	291.22
356	VSN	1442.68	-325	1463	DUMMY	-1385.69	291.22
357	VSN	1481.67	-325	1464	DUMMY	-1733.61	291.22
358	VSN	1520.66	-325	1465	DUMMY	-1781.6	291.22
359	VCL	1559.65	-325	1466	DUMMY	-1829.59	291.22
360	VCL	1598.64	-325	1467	DUMMY	-1877.58	291.22
361	ATEST4_NV	1637.64	-325	1468	DUMMY	-1925.57	291.22
362	VDD	1676.63	-325	1469	DUMMY	-1973.56	291.22
363	VDD	1715.62	-325	1470	DUMMY	-2021.55	291.22
364	VSSD	1754.61	-325	1471	DUMMY	-2069.54	291.22
365	VSSD	1793.6	-325	1472	DUMMY	-2117.53	291.22
366	PSW_ENN	1832.59	-325	1473	DUMMY	-2165.52	291.22
367	PSW_PRIO_SEL	1871.58	-325	1474	DUMMY	-2213.51	291.22
368	VSSD	1910.58	-325	1475	DUMMY	-2261.5	291.22
369	VSSD	1949.57	-325	1476	DUMMY	-2309.49	291.22
370	VSSD	1988.56	-325	1477	DUMMY	-2357.48	291.22
371	VSSD	2027.55	-325	1478	DUMMY	-2405.47	291.22
372	PMOD_SEL	2066.54	-325	1479	DUMMY	-2453.45	291.22

373	IGZO_MOD	2105.53	-325	1480	DUMMY	-2501.44	291.22
374	VSSD	2144.52	-325	1481	DUMMY	-2549.43	291.22
375	VSSD	2183.51	-325	1482	DUMMY	-2597.42	291.22
376	BS<3>	2222.51	-325	1483	DUMMY	-2645.41	291.22
377	BS<2>	2261.5	-325	1484	DUMMY	-2693.4	291.22
378	BS<1>	2300.49	-325	1485	DUMMY	-2741.39	291.22
379	BS<0>	2339.48	-325	1486	DUMMY	-2789.38	291.22
380	IM<3>	2378.47	-325	1487	DUMMY	-2837.37	291.22
381	IM<2>	2417.46	-325	1488	DUMMY	-2885.36	291.22
382	IM<1>	2456.45	-325	1489	DUMMY	-2933.35	291.22
383	IM<0>	2495.45	-325	1490	DUMMY	-2981.34	291.22
384	VSSD	2534.44	-325	1491	DUMMY	-3029.33	291.22
385	VSSD	2573.43	-325	1492	DUMMY	-3077.32	291.22
386	VSSD	2612.42	-325	1493	DUMMY	-3125.31	291.22
387	VSSD	2651.41	-325	1494	DUMMY	-3173.29	291.22
388	CSN_FLH	2690.4	-325	1495	DUMMY	-3221.28	291.22
389	CSN_FLH	2729.39	-325	1496	DUMMY	-3269.27	291.22
390	SCK_FLH	2768.38	-325	1497	DUMMY	-3317.26	291.22
391	SCK_FLH	2807.38	-325	1498	DUMMY	-3365.25	291.22
392	MISO_FLH	2846.37	-325	1499	DUMMY	-3413.24	291.22
393	MISO_FLH	2885.36	-325	1500	DUMMY	-3461.23	291.22
394	MOSI_FLH	2924.35	-325	1501	DUMMY	-3509.22	291.22
395	MOSI_FLH	2963.34	-325	1502	DUMMY	-3557.21	291.22
396	VDDI_FLH	3002.33	-325	1503	DUMMY	-3593.2	191.22
397	VDDI_FLH	3041.32	-325	1504	DUMMY	-3605.2	291.22
398	VDD_TP	3080.32	-325	1505	DUMMY	-3617.2	191.22
399	VDD_TP	3119.31	-325	1506	DUMMY	-3629.19	291.22
400	VSSD	3158.3	-325	1507	DUMMY	-3641.19	191.22
401	VSSD	3197.29	-325	1508	DUMMY	-3653.19	291.22
402	VSSD	3236.28	-325	1509	SX<240>	-3665.19	191.22
403	VSSD	3275.27	-325	1510	S<408>	-3677.18	291.22
404	VSSD	3314.26	-325	1511	S<407>	-3689.18	191.22
405	SCAN_MODE	3353.25	-325	1512	VSSA	-3701.18	291.22
406	SCAN_MODE	3392.25	-325	1513	S<406>	-3713.17	191.22
407	SCAN_EN	3431.24	-325	1514	SX<239>	-3725.17	291.22
408	SCAN_EN	3470.23	-325	1515	S<405>	-3737.17	191.22
409	SCAN_IN<2>	3509.22	-325	1516	S<404>	-3749.17	291.22
410	SCAN_IN<2>	3548.21	-325	1517	VSSA	-3761.16	191.22
411	SCAN_IN<1>	3587.2	-325	1518	S<403>	-3773.16	291.22
412	SCAN_IN<1>	3626.19	-325	1519	SX<238>	-3785.16	191.22
413	SCAN_IN<0>	3665.19	-325	1520	S<402>	-3797.16	291.22
414	SCAN_IN<0>	3704.18	-325	1521	S<401>	-3809.15	191.22
415	SCAN_OUT<2>	3743.17	-325	1522	VSSA	-3821.15	291.22
416	SCAN_OUT<2>	3782.16	-325	1523	S<400>	-3833.15	191.22
417	SCAN_OUT<1>	3821.15	-325	1524	SX<237>	-3845.15	291.22
418	SCAN_OUT<1>	3860.14	-325	1525	S<399>	-3857.14	191.22
419	SCAN_OUT<0>	3899.13	-325	1526	S<398>	-3869.14	291.22

420	SCAN_OUT<0>	3938.12	-325	1527	VSSA	-3881.14	191.22
421	WORK_MODE	3977.12	-325	1528	S<397>	-3893.13	291.22
422	WORK_MODE	4016.11	-325	1529	SX<236>	-3905.13	191.22
423	TS_SEL	4055.1	-325	1530	S<396>	-3917.13	291.22
424	TS_SEL	4094.09	-325	1531	S<395>	-3929.13	191.22
425	RSTN_TP	4133.08	-325	1532	SX<235>	-3941.12	291.22
426	RSTN_TP	4172.07	-325	1533	S<394>	-3953.12	191.22
427	VDDI_TP	4211.06	-325	1534	SX<234>	-3965.12	291.22
428	VDDI_TP	4250.06	-325	1535	S<393>	-3977.12	191.22
429	VDDI_TP	4289.05	-325	1536	S<392>	-3989.11	291.22
430	VDDI_TP	4328.04	-325	1537	SX<233>	-4001.11	191.22
431	VDDI_TP	4367.03	-325	1538	S<391>	-4013.11	291.22
432	VSSD	4406.02	-325	1539	SX<232>	-4025.11	191.22
433	VSSD	4445.01	-325	1540	S<390>	-4037.1	291.22
434	CSN_TP	4484	-325	1541	S<389>	-4049.1	191.22
435	CSN_TP	4522.99	-325	1542	SX<231>	-4061.1	291.22
436	SCK_TP	4561.99	-325	1543	S<388>	-4073.09	191.22
437	SCK_TP	4600.98	-325	1544	SX<230>	-4085.09	291.22
438	MISO_TP	4639.97	-325	1545	S<387>	-4097.09	191.22
439	MISO_TP	4678.96	-325	1546	S<386>	-4109.09	291.22
440	MOSI_TP	4717.95	-325	1547	SX<229>	-4121.08	191.22
441	MOSI_TP	4756.94	-325	1548	S<385>	-4133.08	291.22
442	GPIO<7>	4795.93	-325	1549	SX<228>	-4145.08	191.22
443	GPIO<7>	4834.93	-325	1550	S<384>	-4157.08	291.22
444	VDD_TP	4873.92	-325	1551	S<383>	-4169.07	191.22
445	VDD_TP	4912.91	-325	1552	SX<227>	-4181.07	291.22
446	VSSD	4951.9	-325	1553	S<382>	-4193.07	191.22
447	VSSD	4990.89	-325	1554	SX<226>	-4205.07	291.22
448	VSSD	5029.88	-325	1555	S<381>	-4217.06	191.22
449	GPIO<6>	5068.87	-325	1556	S<380>	-4229.06	291.22
450	GPIO<6>	5107.86	-325	1557	SX<225>	-4241.06	191.22
451	GPIO<5>	5146.86	-325	1558	S<379>	-4253.05	291.22
452	GPIO<5>	5185.85	-325	1559	SX<224>	-4265.05	191.22
453	GPIO<4>	5224.84	-325	1560	S<378>	-4277.05	291.22
454	GPIO<4>	5263.83	-325	1561	S<377>	-4289.05	191.22
455	GPIO<3>	5302.82	-325	1562	VSSA	-4301.04	291.22
456	GPIO<3>	5341.81	-325	1563	S<376>	-4313.04	191.22
457	GPIO<2>	5380.8	-325	1564	SX<223>	-4325.04	291.22
458	GPIO<2>	5419.8	-325	1565	S<375>	-4337.04	191.22
459	GPIO<1>	5458.79	-325	1566	S<374>	-4349.03	291.22
460	GPIO<1>	5497.78	-325	1567	VSSA	-4361.03	191.22
461	GPIO<0>	5536.77	-325	1568	S<373>	-4373.03	291.22
462	GPIO<0>	5575.76	-325	1569	SX<222>	-4385.03	191.22
463	VSSD	5614.75	-325	1570	S<372>	-4397.02	291.22
464	VSSD	5653.74	-325	1571	S<371>	-4409.02	191.22
465	VSSD	5692.73	-325	1572	VSSA	-4421.02	291.22
466	VSSD	5731.73	-325	1573	S<370>	-4433.01	191.22

467	VSSD	5770.72	-325	1574	SX<221>	-4445.01	291.22
468	VSSD	5809.71	-325	1575	S<369>	-4457.01	191.22
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473	VDDI_TP	6004.67	-325	1580	S<366>	-4517	291.22
474	VDDI_TP	6043.66	-325	1581	S<365>	-4528.99	191.22
475	VDD_TP	6082.65	-325	1582	SX<219>	-4540.99	291.22
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489	VSSA	6628.53	-325	1596	S<356>	-4708.95	291.22
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633	VGH	12243.28	-325	1740	VSSA	-6436.57	291.22
634	VGH	12282.27	-325	1741	VSSA	-6448.57	191.22
635	VGHOUT1	12321.26	-325	1742	VSSA	-6460.56	291.22
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637	VGHOUT1	12399.24	-325	1744	VSSA	-6484.56	291.22
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644	VSSA	12039.32	291.22	1751	VSSA	-6568.54	191.22
645	VCOM_PASS_R	12027.33	191.22	1752	VSSA	-6580.54	291.22
646	VCOM_PASS_R	12015.33	291.22	1753	VSSA	-6592.53	191.22
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